PNS SCHOOL OF ENGG. & TECH., MARSHAGHAI
DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING
LESSON PLAN

BRANCH : COMP. SC. & ENGINEERING	SEMESTER : 3RD		NAME OF THE TEACHING FACULTY : MR. ADITYA NARAYAN JENA
SUBJECT : DIGITAL ELECTRONICS	NO. OF DAYS PER WEEK CLASS ALLOTTED : 05		SEMESTER FROM DATE : 15.09.2022 TO 22.12.2022
CHAPTER	**MONTH**	**DATE**	**TOPIC TO BE COVERED**
BASICS OF DIGITAL ELECTRONICS	SEP	15.09.22	NUMBER SYSTEM-BINARY, OCTAL, DECIMAL, HEXADECIMAL NUMBER SYSTEM
		19.09.22	CONVERSION OF BINARY/OCTAL/HEXADECIMAL NUMBER SYSTEM INTO DECIMAL NUMBER SYSTEM
		20.09.22	CONVERSION OF DECIMAL NUMBER SYSTEM INTO BINARY/OCTAL/HEXADECIMAL NUMBER SYSTEM
		21.09.22	CONVERSION OF BINARY TO OCTAL, OCTAL TO BINARY, BINARY TO HEXADECIMAL,HEXADECIMAL NUMBER SYSTEM INTO BINARY NUMBER SYSTEM OCTAL TO HEXADECIMAL, HEXADECIMAL TO OCTAL NUMBER SYSTEM
		22.09.22	BINARY ARITHMATIC (ADDITION,SUBTRACTION,MULTIPLICATION,DIVISION)
		24.09.22	1'S COMPLEMENT,2'S COMPLEMENT AND SUBTRACTION OF BINARY NUMBER USING COMPLEMENT METHOD
		26.09.22	BINARY CODES(BCD,XS-3,GRAY CODE)
		27.09.22	LOGIC GATES(AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR)-SYMBOL,EXPRESSION, TRUTH TABLE AND TIMING DIAGRAM.
		28.09.22	UNIVERSAL GATES AND ITS REALIZATION (USING NAND GATES).
		29.09.22	UNIVERSAL GATES AND ITS REALIZATION (USING NOR GATES).
	OCT	10.10.22	BOOLEAN ALGEBRA, BOOLEAN EXPRESSIONS, DEMORGAN'S THEOREM.
		11.10.22	SOP,STANDARD SOP,MIN TERM
		13.10.22	POS,STANDARD POS,MAX TERM
		15.10.22	2-VARIABLE,3-VARIABLE,4-VARIABLE K-MAP
		18.10.22	SIMPLIFICATION OF SOP AND POS EXPRESSION USING K-MAP
		19.10.22	DON'T CARE CONDITIONS.
COMBINATIONAL LOGIC CIRCUITS	OCT	20.10.22	CONCEPT OF CLC, HALF ADDER WORKING AND LOGIC DIAGRAM
		22.10.22	FULL ADDER WORKING,TRUTH TABLE,LOGIC DIAGRAM
		26.10.22	HALF SUBTRACTOR,FULL SUBTRACTOR WORKING,TRUTH TABLE,LOGIC DIAGRAM
		27.10.22	SERIAL AND PARALLEL BINARY 4-BIT ADDER WORKING
		29.10.22	DECODER,ENCODER
		31.10.22	4:1 MUX,1:4 DMUX WORKING,LOGIC DIAGRAM
	NOV	01.11.22	2-BIT COMPARATOR,3-BIT COMPARATOR WORKING
		02.11.22	SEVEN SEGMENT DECODER(CONCEPT,LOGIC CIRCUIT,TRUTH TABLE,APPLICATION)
SEQUENTIAL LOGIC CIRCUITS	NOV	03.11.22	SLC,TYPES OF SLC,DIFFERENCE BETWEEN CLC AND SLC,CONCEPT OF CLOCK AND TRIGGERING
		05.11.22	NOR BASED SR-FF AND NAND-BASED SR-FF WORKING
		09.11.22	CLOCKED SR FLIP-FLOP,D-FF WORKING
		10.11.22	CLOCKED JK FLIP-FLOP WORKING,CLOCKED T-FF
		12.11.22	RACE AROUND CONDITION,MASTER-SLAVE JK-FF WORKING,APPLICATION OF FLIP-FLOPS

REGISTERS, MEMORIES & PLD	NOV	14.11.22	SHIFT REGISTERS-SERIAL-IN SERIAL-OUT(SIPO) WORKING
		15.11.22	SERIAL-IN PARALLEL-OUT(SIPO)
		17.11.22	CLASS TEST
		19.11.22	PARALLEL-IN SERIAL-OUT (PIPO) WORKING
		21.11.22	PARALLEL-IN PARALLEL-OUT (PIPO) WORKING
		22.11.22	UNIVERSAL SHIFT REGISTER AND ITS APPLICATION.
		24.11.22	DEFINE COUNTER, TYPES OF COUNTER AND ITS APPLICATIONS.
		26.11.22	4-BIT RIPPLE COUNTER WORKING,TIMING DIAGRAM
		28.11.22	BINARY COUNTER WORKING
		29.11.22	DECADE COUNTER WORKING
		30.11.22	SYNCHRONOUS COUNTER WORKING
	DEC	01.12.22	RING COUNTER WORKING
		03.12.22	CONCEPT OF MEMORIES,TYPES
		05.12.22	RAM,STATIC RAM, DYNAMIC RAM
		06.12.22	ROM,ITS TYPES
		07.12.22	BASIC CONCEPT OF PLD, APPLICATION PLD
A/D AND D/A CONVERTERS	DEC	08.12.22	NECESSITY OF A/D AND D/A CONVERTER
		10.12.22	D/A CONVERSION USING WEIGHTED RESISTORS METHOD
		12.12.22	D/A CONVERSION USING R-2R LADDER (WEIGHTED RESISTORS) NETWORK.
		13.12.22	A/D CONVERSION USING COUNTER METHOD
		14.12.22	A/D CONVERSION USING SUCCESSIVE APPROXIMATE METHOD
LOGIC FAMILIES	DEC	15.12.22	VARIOUS LOGIC FAMILIES & TYPES ACCORDING TO THE IC FABRICATION PROCESS.
		17.12.22	CHARACTERISTICS OF DIGITAL ICS-PROPAGATION DELAY, FAN- OUT, FAN-IN.
		19.12.22	POWER DISSIPATION, NOISE MARGIN, POWER SUPPLY REQUIREMENT, AND SPEED WITH REFERENCE TO LOGIC FAMILIES
		20.12.22	FEATURES, CIRCUIT OPERATION;APPLICATIONS OF TTL (NAND)
		21.12.22	FEATURES, CIRCUIT OPERATION; APPLICATIONS OF CMOS (NAND)
		22.12.22	FEATURES, CIRCUIT OPERATION; APPLICATIONS OF CMOS (NOR)

SIGNATURE OF H.O.D.

SIGNATURE OF LECTURER