PNS SCHOOL OF ENGINEERING &TECHNOLOGY

NISAMANI VIHAR, MARSHAGHAI, KENDRAPARA

DEPARTEMENT OF ELECTRONICS & TELECOMMUNICATION ENGINEERING

1ST INTERNAL ASSESSMENT EXAM QUESTIONS & ANSWER

SUB-DIGITAL ELECTRONICS (TH-3)

PREPARED BY :

ER. ADITYA NARAYAN JENA

LECTURER IN ETC

PNS School of Engineering & Technology

Nishamani Vihar, Marshaghai, Kendrapara

Internal Assessment Examination-2022(3rd Semester)

Subject : Th-3 -Digital Electronics

Branch : Computer Science & ETC Engineering

Time : $1\frac{1}{2}$ Hours F.M. : 20

1. Answer all questions [2 x 5]

(a) What do you mean by base of a number system ?

(b) Convert $(276)_8$ into $(\_\_\_\_\_\_)_{16}$?

(c) Find 2's Complement of $(11.01)_2$.

(d) Define min term and max term.

(e) Draw the gate symbol and truth table of 3 input NAND gate.

2. Answer any two questions. [5 x 2]

(a) State and prove De-Morgan's Theorem.

(b) Explain the working principle of full Adder with Truth Table and Logic Diagram.

(c) Solve by K-map :

$$F(A,B,C,D) = \Sigma m(1,3,7,11,15) + d(0, 2, 5)$$

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1- (a) Base of a number system ÷

The number of digits used in a number system is known as base of that no. system.

For eg; The base of binary no. system is 2,since only 0 & 1 used in Binary number system.

(b) $(276)_8$

$= (010111110)_2$

$=(0000\ 1011\ 1110)_{16} = (OBE)_{16}$ (Ans)

(c) $(11.01)_2$

1's complement = 00 . 10

2's complement = 00 . 10

+ 1

$(00.11) = (00.11)_2$ (Ans)

(d) Min term ÷

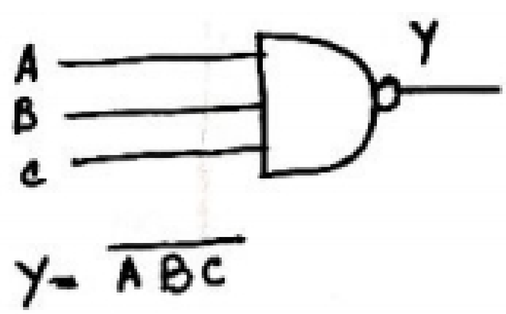
In SOP expression, the term which contains all the variables in direct or complement form , is known as min term.

Max term÷

In POS expression , the term which contains all the variable in direct or complement form , is known as max term.

(e) <u>3 input NAND gate</u> ÷

Gate symbol -



Truth table -

Input			Output
A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

2- <u>(a) Demorgan's Theorem ÷</u>

(I) $\overline{X+Y} = \overline{X} \,.\, \overline{Y}$

(II) $\overline{X.Y} = \overline{X} + \overline{Y}$

Where x , y are two logic variables

<u>proof</u>

(i) $\overline{X+Y} = \overline{X} \,.\, \overline{Y}$

<u>Truth table ÷</u>

X	Y	X+Y	$\overline{X+Y}$	$\overline{X}$	$\overline{Y}$	$\overline{X}\,.\overline{Y}$
0	0	0	1	1	1	1
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	O	0	0	0

From truth table $\overline{X+Y} = \overline{X}\,.\overline{Y}$ (Proved)

(ii) $\overline{X.Y} = \overline{x} + \overline{y}$

Truth table ÷

X	Y	X.Y	$\overline{X.Y}$	$\overline{X}$	$\overline{Y}$	$\overline{X}+\overline{y}$
0	0	0	1	1	1	1
0	1	0	1	1	0	1
1	0	0	1	0	1	1
1	1	1	0	0	0	0

From truth table, $\overline{X.Y}= \overline{X} + \overline{Y}$ (Proved)

2 (b)

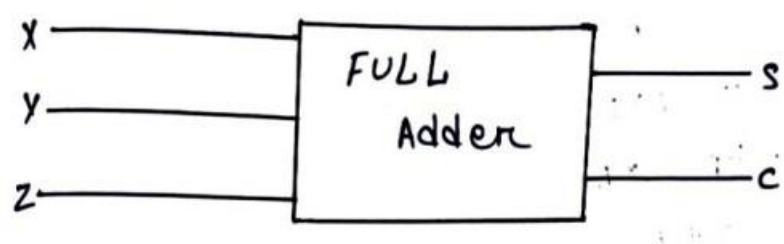
FULL ADDER ÷

It is a combinational logic circuit which perform the arithimatic addition of only 3 binary bits.

- Here no of inputs = 3 i.e x,y and z; and no of output = 2 i.e s,c

Where S = Sum

C = Carry



<BD of a full adder>

Truth Table ÷

Input			Output	
x	y	z	s	c
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Expression for s ÷

x \ yz	00	01	11	10
0		1		1
1	1		1	

$S = \bar{x}\,\bar{y}\,z + \bar{x}\,y\,\bar{z} + x\,\bar{y}\,\bar{z} + x\,y\,z$

$= \bar{x}\,(\bar{y}\,z + y\,\bar{z}) + x\,(\bar{y}\,\bar{z} + y\,z)$

Let

$\bar{y}\,z + y\,\bar{z} = A$

$\bar{A} = y\,\bar{z} + y\bar{z}$

$S = \bar{X}\,A + X\bar{A}$

$= x \oplus A$

$= x \oplus (\bar{y}\,z + y\,\bar{z})$

$= x \oplus y \oplus z$

Expression for c÷

x \ yz	00	01	11	10
0	00	01	1	10
1		1	1	1

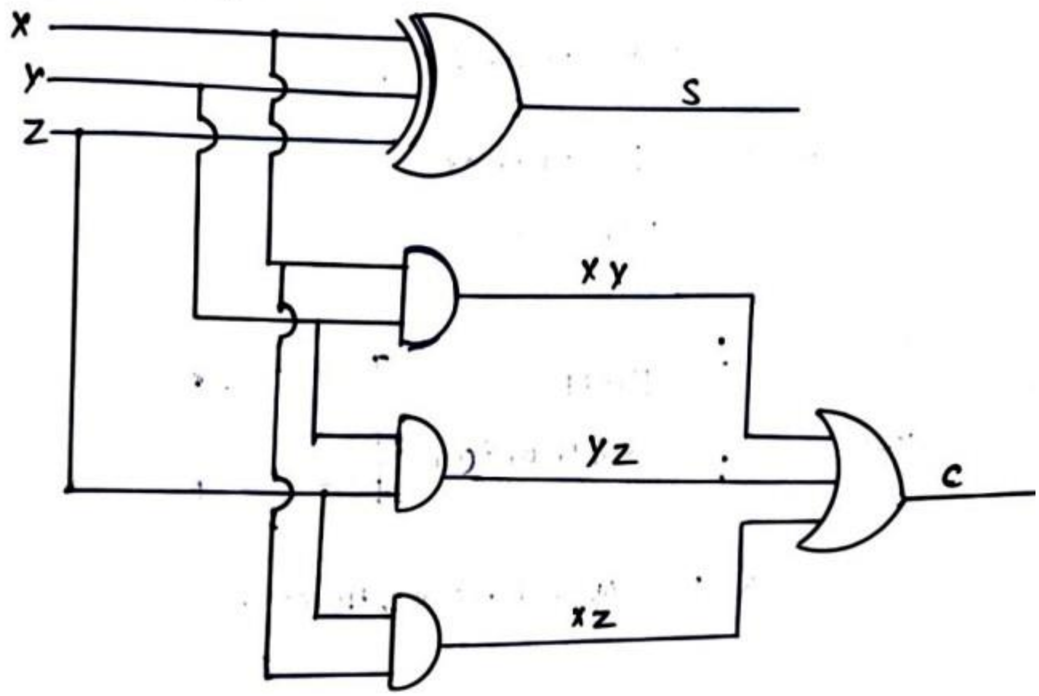
C= y z +x z+ y x

=x y +y z+ x z

Logic diagram of full odder÷

$S = x \oplus y \oplus z$

$C = x\,y + y\,z + x\,z$



2- (C) Solve by k-map

$F(A, B, C, D) = \sum_m (1,3,7,11,15) + d(0, 2\ 5)$

AB \ CD	00	01	11	10
00	×	1	1	×
01		×	1	
11			1	
10			1	

$F = \overline{A}\ \overline{B} + C\,D$ (ans)