PNS SCHOOL OF ENGINEERING & TECHNOLOGY

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DEPARTMENT OF ELECTRONICS & TELECOMMUNICATION ENGINEERING

1ST INTERNAL ASSESSMENT EXAM QUESTIONS & ANSWER

SUB-VLSI & EMBEDDED SYSTEM (TH-2)

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Internal Assessment Examination-2022(5th Semester)

Subject : Th-2 -VLSI & Embedded System

Branch : ETC Engineering

Time : $1\frac{1}{2}$ Hours F.M. : 20

1. Answer ALL the questions. [2 x 5]

   (a) Define Modularity.

   (b) Classify VLSI design style.

   (c) Define FPGA.

   (d) Write down the 3 domains present in y-chart.

   (e) Implement y = AB+C, using CMOS logic ckt.

2. Answer the following questions. (any Two) [5 x 2]

   (a) Explain briefly the VLSI design methodologies.

   (b) Explain the VLSI design flow and y-chart in details.

   (c) Explain the Fabrication Process of NMOS transistor.

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1- (a) Modularity÷

- It allows each block or module can be designed relatively independently form each other.
- The various functional blocks which make the large system must have well defined functions & interfaces .

(b) VLSI design style÷

VLSI design style are of 2 types.

- Full custom design style
- Semi custom design style

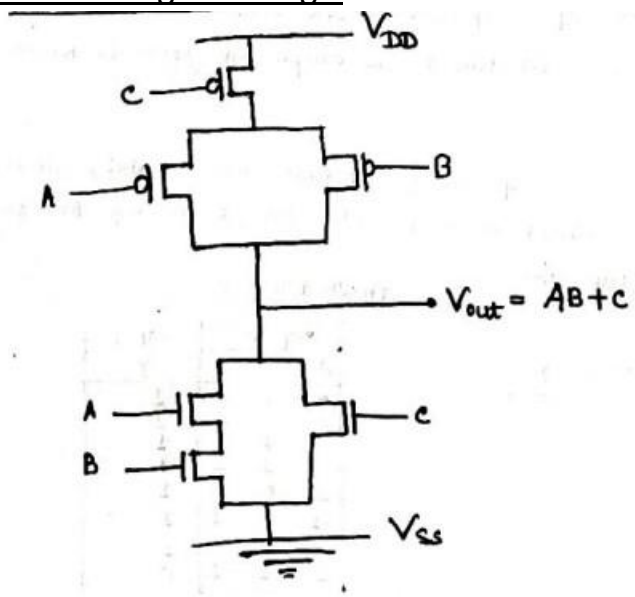
(c) FPGA÷

- It stands for Field Programmable Gate Array.
- FPGA consists of I/O buffers, configurable logic blocks(CLBs) and programmable interconnect structure.

(d) Y-chart ÷

3 domains are present in y-chart.
(a) Behavioural domain
(b) structural domain
(c) Geometrical layout domain

(e) Y= A+B+C using cmos logic ÷



2-a)VLSI DESIGN METHODOLOGIES:-

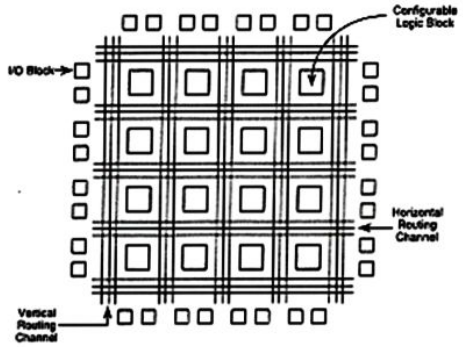
Full Custom Design

- Although the standard-cells based design is often called full custom design, in a strict sense, it is somewhat less than fully custom since the cells are pre-designed for general use and the same cells are utilized in many different chip designs.
- In a full custom design, the entire mask design is done anew without use of any library. However, the development cost of such a design style is becoming prohibitively high. Thus, the concept of design reuse is becoming popular in order to reduce design cycle time and development cost.
- The most rigorous full custom design can be the design of a memory cell, be it static or dynamic. Since the same layout design is replicated, there would not be any alternative to high density memory chip design.
- For logic chip design, a good compromise can be achieved by using a combination of different design styles on the same chip, such as standard cells, data-path cells and PLAs. In real full-custom layout in which the geometry, orientation and placement of every transistor is done individually by the designer, design productivity is usually very low - typically 10 to 20 transistors per day, per designer.
- In digital CMOS VLSI, full-custom design is rarely used due to the high labor cost. Exceptions to this include the design of high-volume products such as memory chips, high- performance microprocessors and FPGA masters.

Semicustom design style:-

Field Programmable Gate Array (FPGA)

- Fully fabricated FPGA chips containing thousands of logic gates or even more, with programmable interconnects, are available to users for their custom hardware programming to realize desired functionality.
- This design style provides a means for fast prototyping and also for cost-effective chip design, especially for low-volume applications.
- A typical field programmable gate array (FPGA) chip consists of I/O buffers, an array of configurable logic blocks (CLBs), and programmable interconnect structures. The programming of the interconnects is implemented by programming of RAM cells whose output terminals are connected to the gates of MOS pass transistors.



- The CLB is configured such that many different logic functions can be realized by programming its array.
- The typical design flow of an FPGA chip starts with the behavioral description of its functionality, using a hardware description language such as VHDL. The synthesized architecture is then technology-mapped (or partitioned) into circuits or logic cells.
- At this stage, the chip design is completely described in terms of available logic cells. Next, the placement and routing step assigns individual logic cells to FPGA sites (CLBs) and determines the routing patterns among the cells in accordance with the netlist.
- After routing is completed_performance of the design can be simulated and verified before downloading the design for programming of the FPGA chip. The programming of the chip remains valid as long as the chip is powered-on, or until new programming is done. In most cases, full utilization of the FPGA chip area is not possible - many cell sites may remain unused.

Gate Array Design

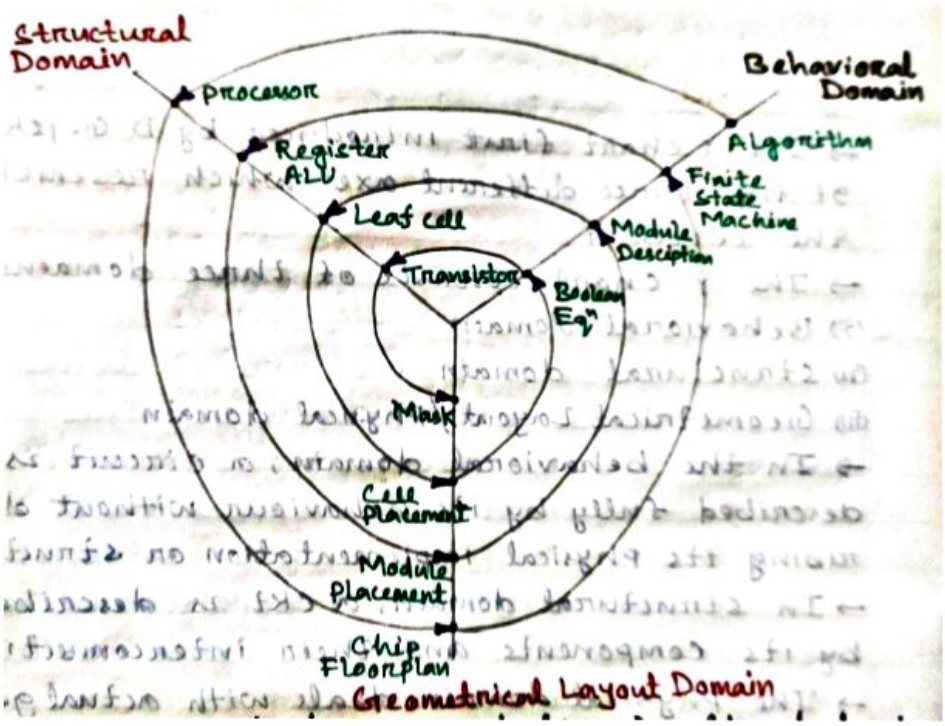
- In view of the fast prototyping capability, the gate array (GA) comes after the FPGA. While the design implementation of the FPGA chip is done with user programming, that of the gate array is done with metal mask design and processing.
- Gate array implementation requires a two-step manufacturing process: The first phase, which is based on generic (standard) masks, results in an array of uncommitted transistors on each GA chip.
- In the second phase these uncommitted chips can be stored for later customization, which is completed by defining the metal interconnects between the transistors of the array.
- Since the patterning of metallic interconnects is done at the end of the chip fabrication, the turn-around time can be still short, a few days to a few weeks.

Standard-Cells Based Design

- The standard-cells based design is one of the most prevalent full custom design styles which require development of a full custom mask set. The standard cell is also called the poly cell.
- In this design style, all of the commonly used logic cells are developed, characterized, and stored in a standard cell library. A typical library may contain a few hundred cells including inverters, NAND gates, NOR gates, complex AOI, OAI gates, D-latches, and flip-flops.
- Each gate type can have multiple implementations to provide adequate driving capability for different fan outs. For instance, the inverter gate can have standard size transistors, double size transistors, and quadruple size transistors so that the chip designer can choose the proper size to achieve high circuit speed and layout density.

2-b) VLSI DESIGN FLOW:-

Y CHART-



The Y-chart consists of three major domains, namely:

- behavioral domain
- structural domain
- Geometrical layout domain

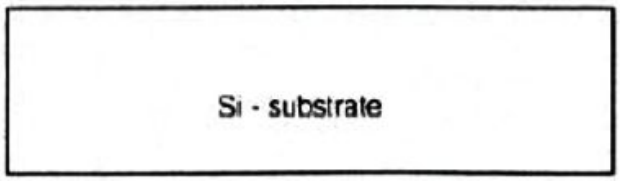
- The design flow starts from the algorithm that describes the behavior of the target chip. The corresponding architecture of the processor is first defined.
- It is mapped onto the chip surface by floor planning.
- The next design evolution in the behavioral domain defines finite state machines (FSMs) which are structurally implemented with functional modules such as registers and arithmetic logic units (ALUs).
- These modules are then geometrically placed onto the chip surface using CAD tools for automatic module placement followed by routing, with a goal of minimizing the interconnects area and signal delays.
- The third evolution starts with a behavioral module description. Individual modules are then implemented with leaf cells.
- At this stage the chip is described in terms of logic gates (leaf cells), which can be placed and interconnected by using a cell placement & routing program.
- The last evolution involves a detailed Boolean description of leaf cells followed by a transistor level implementation of leaf cells and mask generation.
- In standard-cell based design, leaf cells are already pre-designed and stored in a library for logic design use.

2-C)

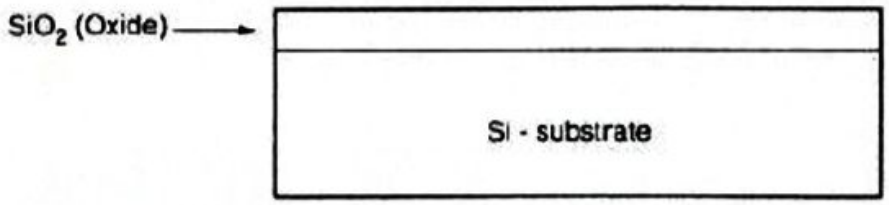
nMOS FABRICATION

Fabrication is the process to create the devices and wires on a single silicon chip.

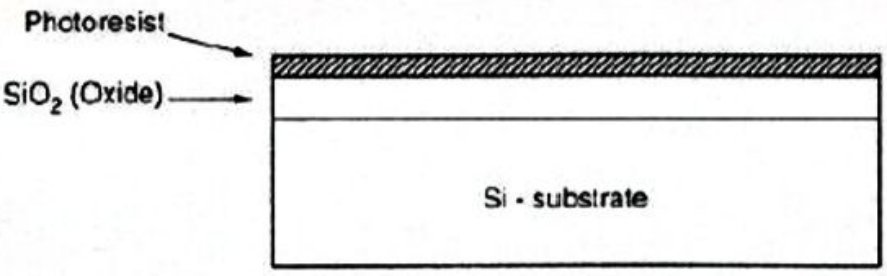
•The process starts with a silicon substrate of high purity into which the required p-impurities are introduced.



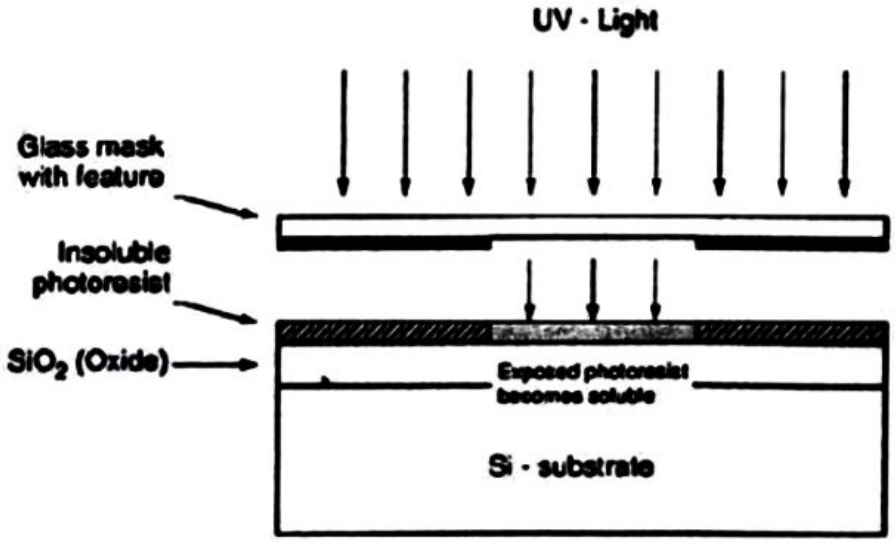
•A layer of silicon dioxide(sio_2) is grown all over the surface of the wafer to protect the surface and acts as a barrier to dopants during processing and provide a generally insulating substrate onto which other layers may be deposited and patterned.



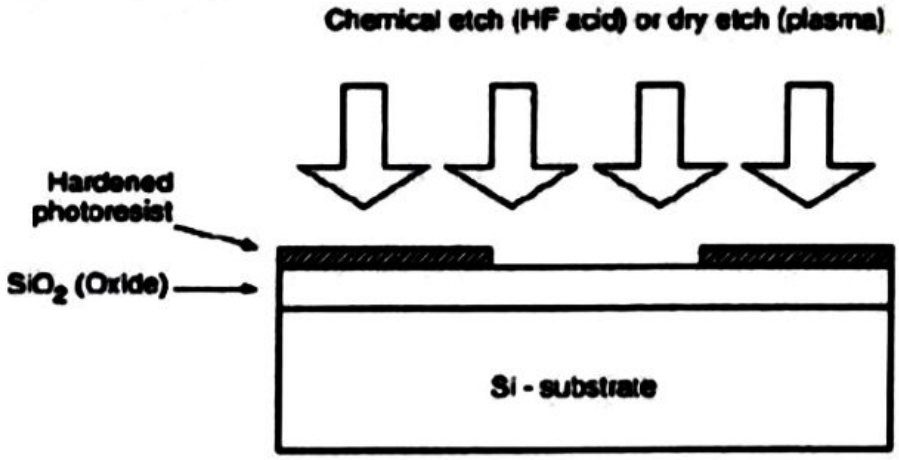
- The surface is now covered with a photoresist which is deposited onto the wafer and spun to achieve an even distribution of the required thickness.



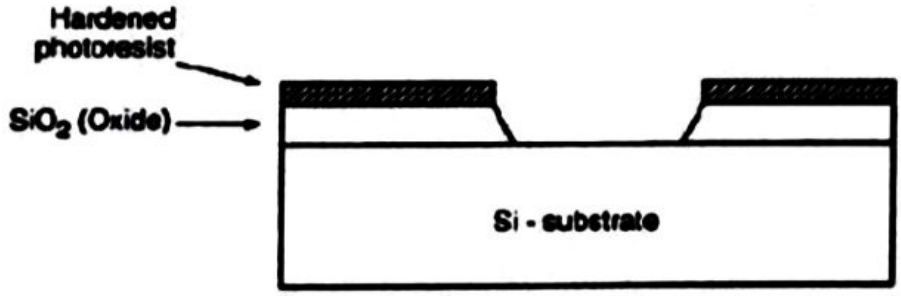
- The photoresist layer is then exposed to ultraviolet light through a mask which efines those regions into which diffusion is to take place together with transistor channels.



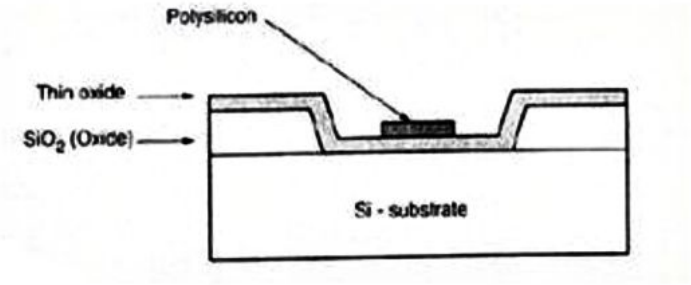
•These areas are subsequently readily etched away together with the underlying silicon dioxide so that the wafer surface is exposed in the window defined by the mask.



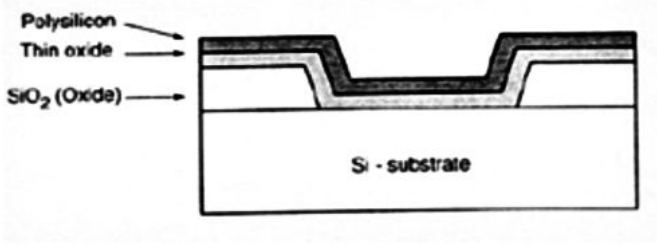
•The remaining photoresist is removed and a thin layer of sio_2 is grown over the entire chip surface and then polysilicon is deposited on top of this to form the gate structure.



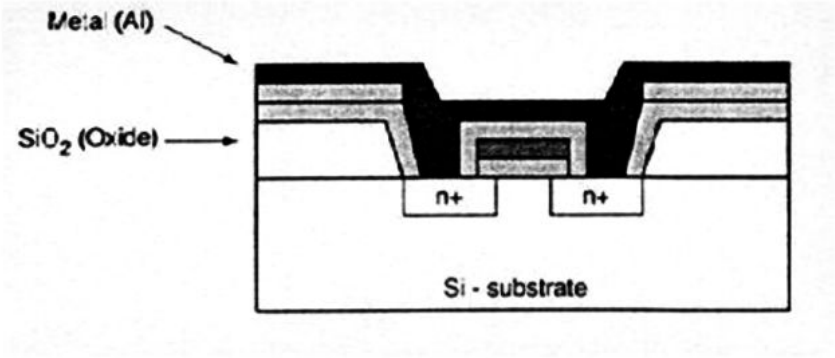
•The polysilicon layer consists of heavily doped polysilicon deposited by chemical vapour deposition(CVD),



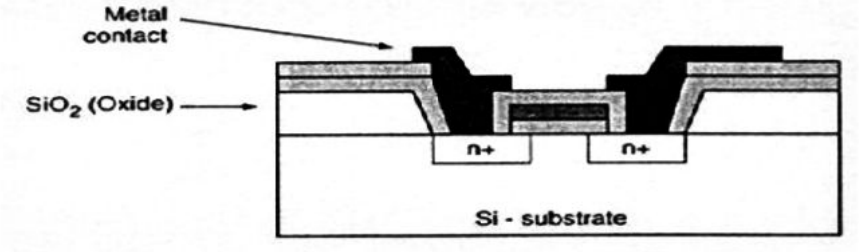
•Further photoresist coating and masking allows the polysilicon to be patterned and then the thin oxide is removed to exposed areas into which n-type impurities are to be diffused to form the source and drain.



•Diffusion is achieved by heating the wafer to a high temperature and passing a gas containing the desired n-type impurity over the surface.



•Thick oxide (sio_2) is grown over all again and is then masked with photoresist and etched to expose selected aareas of the polysilicon gate and the drain and source areas where connections area to be made.



•The whole chip then has metal deposited over the surface to a thickness typically of 1μm. This metal layer is then masked and etched to form the required interconnection pattern.