PNS SCHOOL OF ENGINEERING & TECHNOLOGY

DEPARTMENT OF ELECTRONICSAND TELECOMMUNICATION ENGINEERING

QUESTION BANK

ON

VLSI & EMBEDDED SYSTEM

5TH SEMESTER

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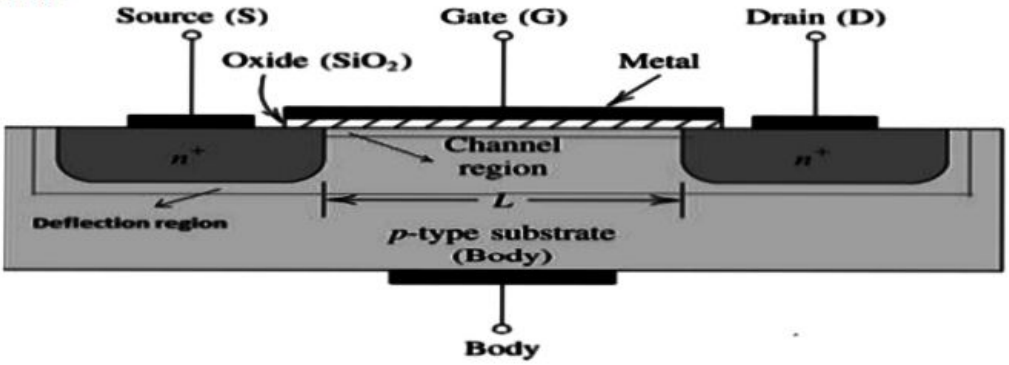
Q-1-a) What is lithography.

ANS:

Lithography is the process of transferring patterns of geometric shapes on a mask to a thin layer of radiation sensitive material known as resist covering the whole surface of the semiconductor substrate.

Q-1-b) Describe operation of MOSFET (any one type) [2018(S)], [2018(W)]

ANS



The aim of the MOSFET is to be able to control the voltage and current flow between the source and drain. It works almost as a switch. The working of MOSFET depends upon the MOS capacitor. The MOS capacitor is the main part of MOSFET. The semiconductor surface at the below oxide layer which is located between source and drain terminal. It can be inverted from p-type to n-type by applying positive or negative gate voltages respectively. When we apply the positive gate voltage the holes present under the oxide layer with a repulsive force and holes are pushed downward with the substrate. The depletion region populated by the bound negative charges which are associated with the acceptor atoms. The electrons reach channel is formed. The positive voltage also attracts electrons from the n+ source and drain regions into the channel. Now, if a voltage is applied between the drain and source, the current flows freely between the source and drain and the gate voltage controls the electrons in the channel. Instead of positive voltage if we apply negative voltage, a hole channel will be formed under the oxide layer.

Q-1-c) Describe different steps of NMOS Fabrication process.

ANS:-

The fabrication steps are as follows:

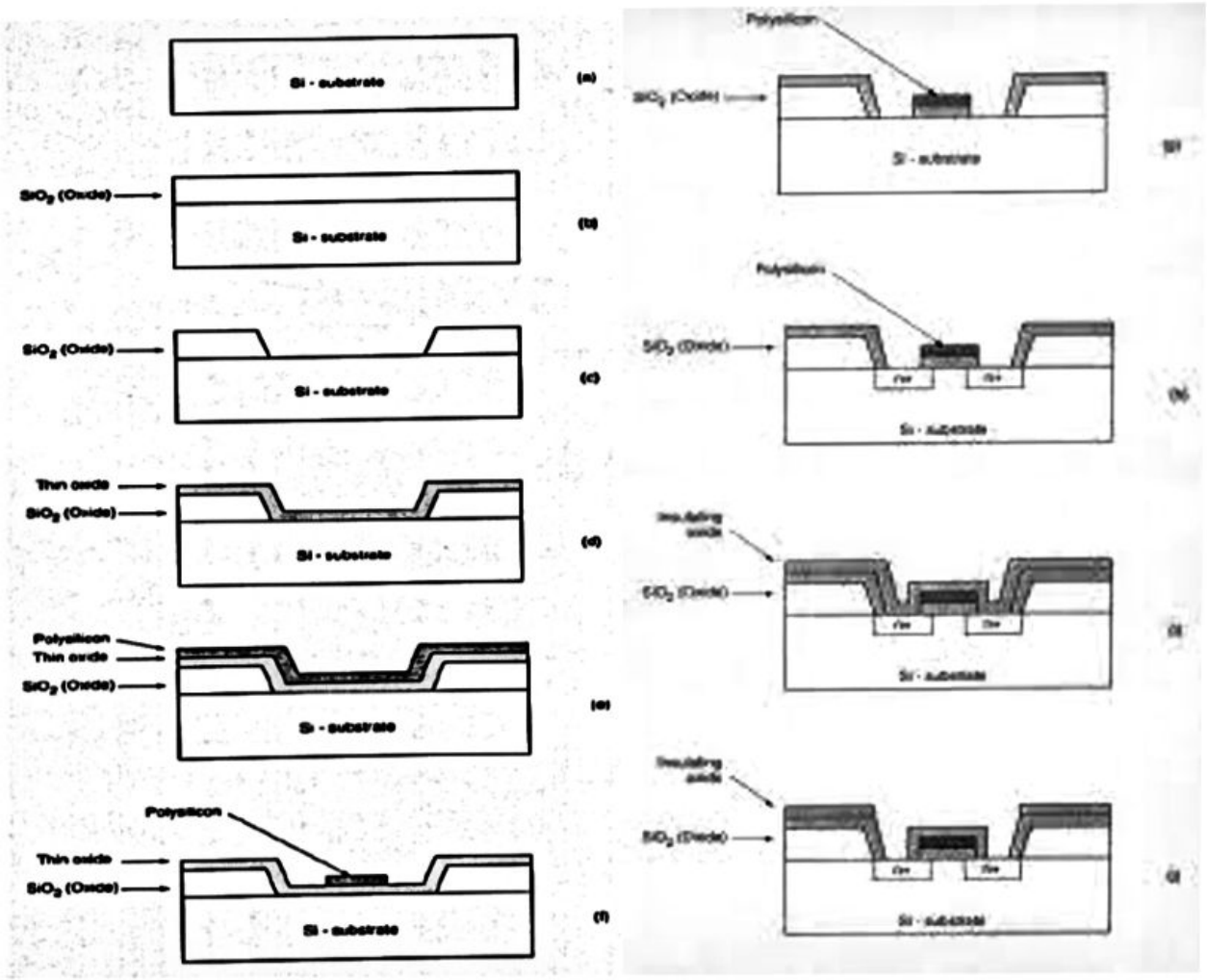
Step1:

Processing is carried on single crystal silicon of high purity on which required P impurities are introduced as crystal is grown. Such wafers are about 75 to 150 mm in diameter and 0.4 mm thick and they are doped with say boron to impurity concentration of 10 to power 15/cm3 to 10 to the power 16 /cm3.

Step 2 :

A layer of silicon di oxide (SiO2) typically 1 micrometer thick is grown all over the surface of the wafer to protect the surface, acts as a barrier to the dopant during processing, and provides a generally insulating substrate on to which other layers may be deposited and patterned.

Step 3:
The surface is now covered with the photo resist which is deposited onto the wafer and spun to an even distribution of the required thickness.



Step 4:
The photo resist layer is then exposed to ultraviolet light through masking which defines those regions into which diffusion is to take place together with transistor channels. Assume, for example , that those areas exposed to uv radiations are polymerized (hardened), but that the areas required for diffusion are shielded by the mask and remain unaffected.

Step 5:
These areas are subsequently readily etched away together with the underlying silicon di oxide so that the wafer surface is exposed in the window defined by the mask.

Step 6:
The remaining photo resist is removed and a thin layer of SiO2 (0.1 micro m typical) is grown over the entire chip surface and then poly silicon is deposited on the top of this to form the gate structure. The polysilicon layer consists of heavily doped polysilicon deposited by chemical vapor deposition (CVD). In the fabrication of fine pattern devices, precise control of thickness, impurity concentration, and resistivity is necessary

Step 7:

Further photo resist coating and masking allows the poly silicon to be patterned and then the thin oxide is removed to expose areas into which n-type impurities are to be diffused to form the source and drain. Diffusion is achieved by heating the wafer to a high temperature and passing a gas containing the desired n-type impurity.

The poly silicon with underlying thin oxide and the thick oxide acts as mask during diffusion the process is self-aligning.

Step 8:

Thick oxide (SiO_2) is grown over all again and is then masked with photo resist and etched to expose selected areas of the poly silicon gate and the drain and source areas where connections are to be made. (Contacts cut)

Step 9:

The whole chip then has metal (aluminum) deposited over its surface to a thickness typically of 1 micro m. This metal layer is then masked and etched to form the required interconnection pattern.

Q-2-a) What is threshold voltage

ANS

The threshold voltage, commonly abbreviated as V_{th}, of a MOSFET is the minimum gate-to-source voltage VGS that is needed to create a conducting path (channel) between the source and drain terminals.

Q-2-b) Explain the Level-1 modeling of MOS transistor.

ANS

The LEVEL-1 model is the simplest current-voltage description of the MOSFET, which is basically the GCA based quadratic model originally conceived by Sah in the early 1960s and later developed by Schichman and Hodges. The equations used for LEVEL-1 n-channel MOSFET model is SPICE is as follows-

Linear region- $I_D = \frac{K'}{2} \cdot \frac{W}{Leff} \cdot [2.(Vgs - Vt)Vds - Vds^2] \cdot (1 + \lambda Vds)$

for $V_{gs} \geq V_t$ and $V_{ds} < V_{gs} - V_t$

Saturation region- $I_D = \frac{K'}{2} \cdot \frac{W}{Leff} .(Vgs - Vt)^2 . (1 + \lambda Vds)$

for $V_{gs} \geq V_t$ and $V_{ds} \geq V_{gs} - V_t$

Where the threshold voltage $V_t = V_{to} + \gamma (\sqrt{|2\varphi f|} - \sqrt{|2\varphi f|})$

The effective channel length $L_{eff} = L - 2L_D$

The empirical channel length modulation term = $(1 + \lambda Vds)$

The physical parameters are $K' = \mu . C_{ox}$, where $C_{ox} = \frac{\varepsilon ox}{tox}$; $\gamma = \frac{\sqrt{2.\varepsilon si.q.Na}}{Cox}$ and

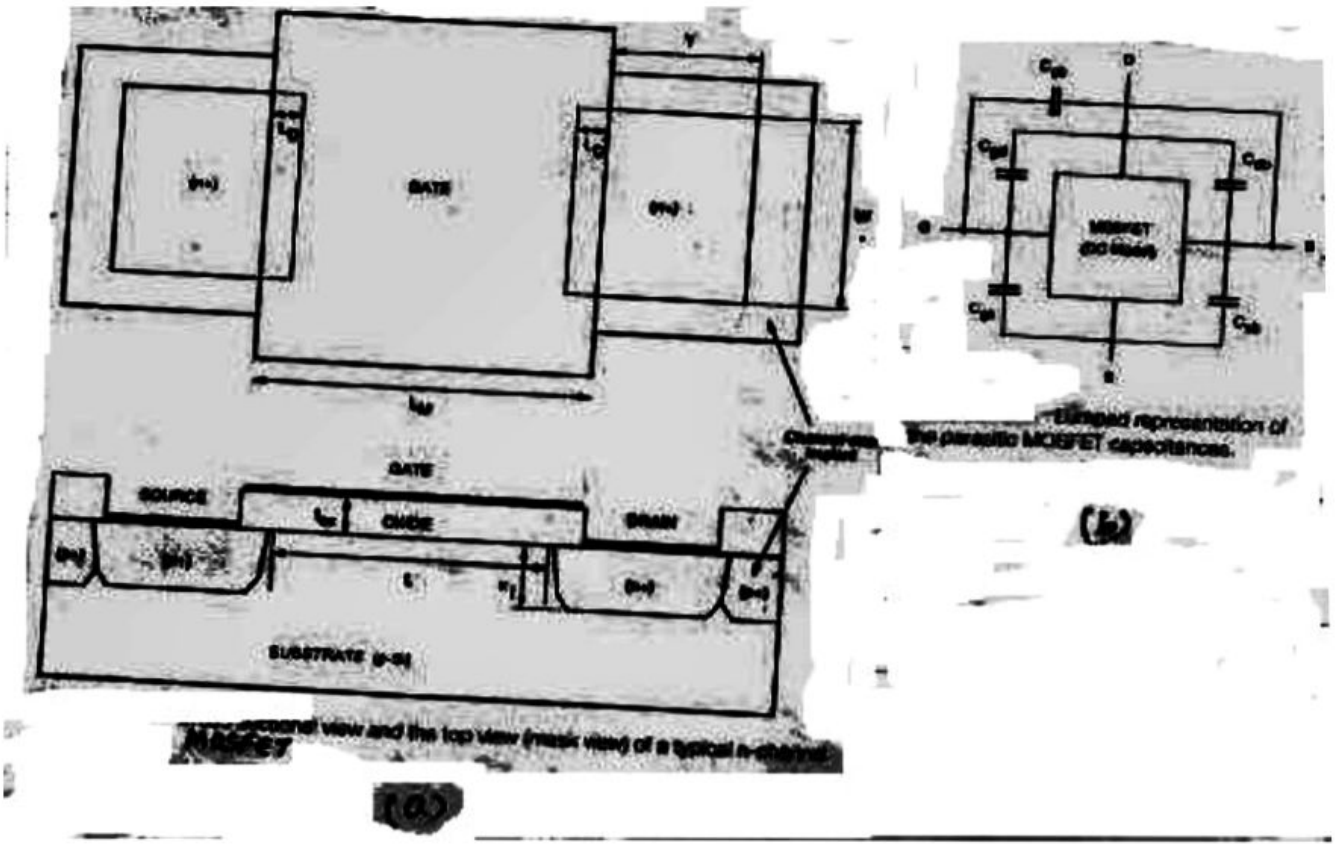
$2\varphi f = 2.\frac{KT}{q} . \ln (\frac{ni}{Na})$

Q-2-c) Explain briefly MOSFET capacitance with neat diagram.

ANS

The on chip capacitances found in MOS circuit are in general complicated functions of the layout geometries and the manufacturing processes. Most of these capacitances are not lumped, but distributed.

The figure-A below shows the cross sectional view and top view of a typical n-channel MOSFET. In this figure, the mask length (drain length) of the gate is L_m, and the actual channel length is L. The extent of both the gate-source and gate-drain overlap are L_D; thus, the channel length is given by – $L = L_m - 2.L_D$

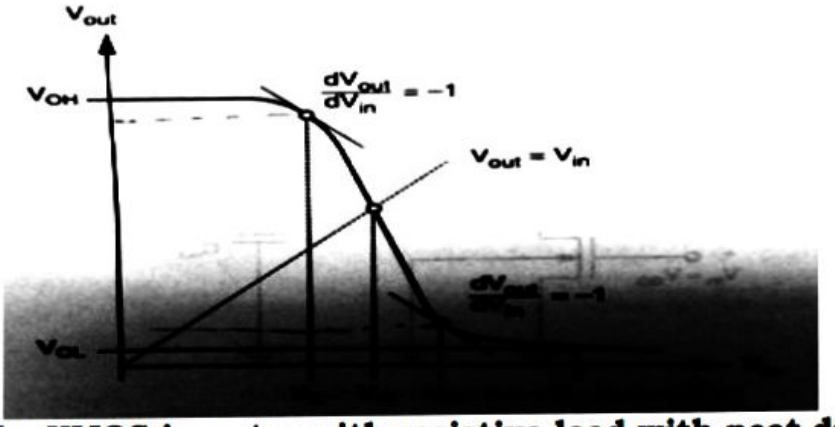


Here, the source and drain overlap region length are equal because of the symmetry of the MOSFET structure (L_D) is on the order of 0.1μm. Both the source and drain diffusion regions have a width of W. The diffusion region length is Y. Here, both source and drain diffusion region are surrounded by a p^+ doped region called the channel stop implant. This additional p^+ region prevent the formation of any unwanted (parasitic) channel between two neighboring n^+ diffusion regions and act to electrically isolate neighboring devices built on the same substrate.

The parasitic capacitances can be identified associated with typical MOSFET structure as lumped equivalent capacitances observed between the device terminals as shown in figure-B; since such a lumped representation can be easily used to analyze the dynamic transient behavior of the device.

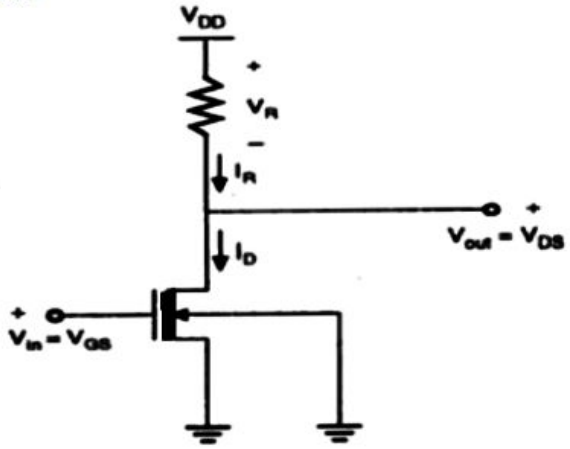
Q-3-a) Draw VTC curve.

ANS



Q-3-b) Describe NMOS inverter with resistive load with neat diagram. [2018(S)], [2018(W)]

ANS



The basic structure of the resistive load inverter is given above.

An enhancement type nMOS transistor acts as the driver device. The load consist of a simple linear resistor R_L. The power supply of the ckt.is V_{DD}. The o/p or drain current I_D is equal to the load current I_R in DC steady state operation. The channel length modulation effect will be neglected (i.e) $\lambda = 0$. As the source and substrate are grounded, hence, $V_{SB} = 0$. Consequently, threshold voltage of the driver transistor is always equal to V_{T0}.

For the input voltage smaller than the threshold voltage V_{T0}, the transistor is in cut-off (when $V_{in} < V_{T0}$), and does not conduct any current. Since, the voltage drop at load resistor is zero, the o/p voltage must be equal to the power supply voltage, V_{DD}. As the input voltage is increased beyond V_{T0}($V_{T0} \leq V_{in} \leq V_{out} + V_{T0}$), the driver transistor starts conducting a non-zero drain current. The driver MOSFET is at saturation mode as the o/p voltage ($V_{out} = V_{DS}$) is larger than ($V_{in} - V_{T0}$). Thus the resistance current I_R is as $-I_R = \frac{Kn}{2} . (V_{in} - V_{T0})^2$

With increasing input voltage, the drain current of the driver also increases and the o/p voltage Vout starts to drop. Eventually, for input voltage larger than $V_{out} + V_{T0}$, the driver transistor enters the linear operation region ($V_{in} \geq V^{out} + V_{T0}$), as the o/p voltage continues to decrease.

$$\text{So, } I_R = \frac{Kn}{2} . [2.(V_{in} - V_{T0}).V_{out} - V^2_{out}]$$

Q-3-c) Explain dynamic RAM, SRAM and Flash memory.

ANS

- Dynamic random-access memory (DRAM) is a type of storage that is widely used as the main memory for a computer system. DRAM is a type of RAM that stores each bit of data in a separate capacitor within an IC. The capacitor can be either charged or discharged; these two states are taken to represent the two values of a bit, conventionally called 0 and 1. A DRAM storage cell is dynamic in that it needs to be refreshed or given a new electronic charge every few milliseconds to compensate for charge leaks from the capacitor. DRAM is used for main memory. It is slower, large is size and cheaper and consume high power consisting of one transistor.
- Static random-access memory (SRAM) is a type of RAM which is made up of CMOS technology and uses six transistors. It retains data bits in its memory as long as power is being supplied. Unlike the DRAM, which stores bits in cells consisting of a capacitor and a transistor, SRAM does not have to be periodically refreshed. SRAM uses transistors and latches in construction. SRAM is faster than DRAM and used for cache memory.
- Flash memory is one type of ROM similar to EEPROM where data in the block can be erased by using a high electrical voltage. The Flash memory cell consists of one transistor with floating point gate, whose threshold voltage can be changed repeatedly by applying an electric field to its gate. It is a non-volatile computer storage device.

Q-4-a) Whatare different layout design Rule?[2018(S)]

ANS

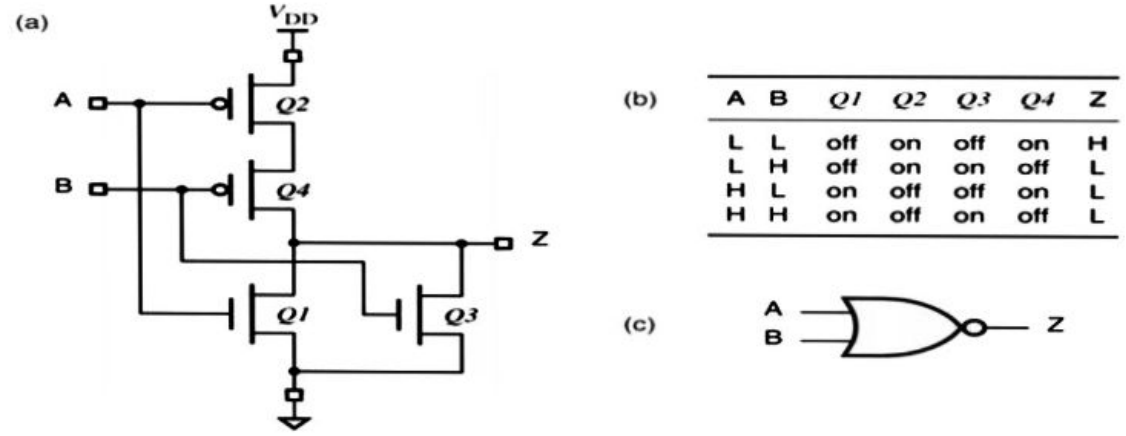
The physical mask layout of any circuit to be manufactured using a particular process must confirm to a set of geometric constants or rules, which are generally called as layout design rules. Usually, these are describe in two way –

(i) Micron rule

(ii) Lambda (λ) rule

Q-4-b) Design CMOS NOR gate with neat diagram. Explain it. [2018(S)], [2018(W)]

ANS



A	B	Q1	Q2	Q3	Q4	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	L
H	L	on	off	off	on	L
H	H	on	off	on	off	L

The circuit diagram of a two input CMOS NOR gate is shown in the above figure-A. The drivers are parallel connected but the loads are series connected.

When either A or B are logic 1, the output is grounded. No path is allowed between the output node and the power supply voltage since the driver is an nMOS device. By placing the load in series, if either or both inputs are at logic 1, one or both load switch remains open. Similarly if both inputs are at logic 0, both load switches are closed providing a path from the output node to V_{DD} since the load is a pMOS device.

The output voltage of CMOS NOR gate will be either logic low voltage of V_{OL}=0 or a logic high voltage of $V_{OH}=V_{DD}$. The switching threshold voltage is an important parameter in determining the device operation. Assuming –

$$\left(\frac{W}{L}\right)_{n,A} = \left(\frac{W}{L}\right)_{n,B} = \left(\frac{W}{L}\right)_{p,A} = \left(\frac{W}{L}\right)_{p,B} \text{and } V_A = V_B = V_{out} = V_{th}$$

At threshold the two parallel nMOS transistors are saturated as $V_{GS} = V_{DS}(V_{in} = V_{out})$. The combined drain current of two nMOS transistors is $(V_{GS} = V_{DS} = V_{th})$: $I_D = K_n(V_{th} - V_{T,n})^2$

$$\text{Or } \boxed{V_{th} = V_{T,n} + \sqrt{\frac{ID}{Kn}}}$$

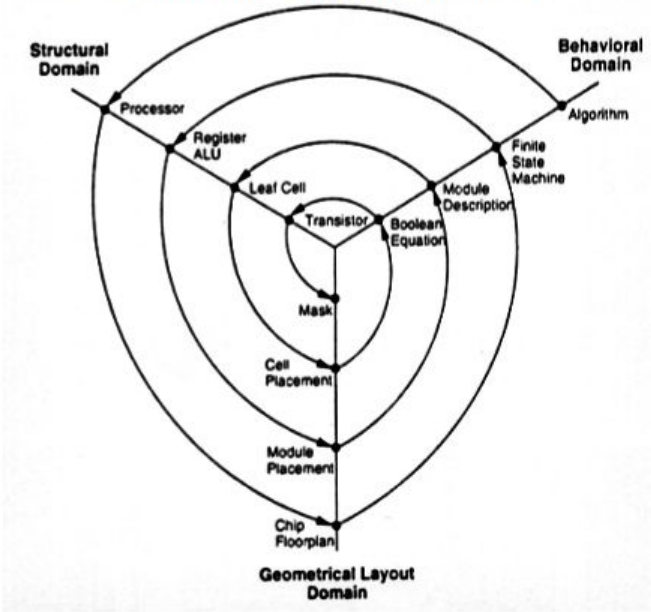
At this time $pMOS_A$ is in linear region and $pMOS_B$ is in saturation. So,

Q-4-c) Describe VLSI design flow by Y-chart method.

ANS

The Y-chart illustrates a simplified design flow for most logic chips, using design activities on three different axes (domain) which reasonable the letter 'Y'. The Y-chart consists of three domains of representation –

1. Behavioral domain
2. Structural domain
3. Geometrical layout domain



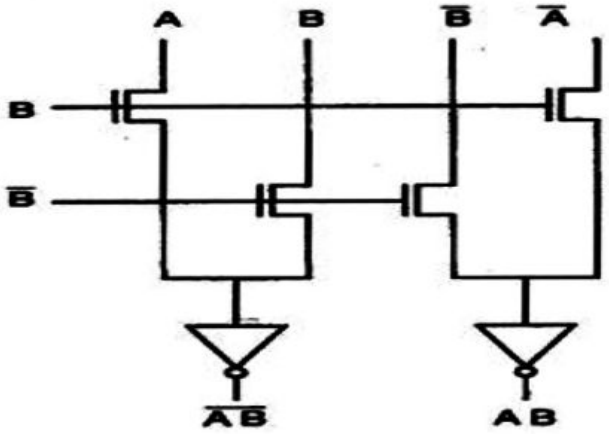
Which are structurally implemented with functional modules such as registers and ALUs. These modules are then geometrically placed into the chip surface using CAD tools for automatic module placement followed by routing, with

a goal of minimizing the interconnects area and signal delays. The third evolution starts with a behavioral module description.

Individual modules are then implemented with leaf cells. At this stage the chip is described in terms of logic gates (leaf cells), which can be placed and interconnected by using a cell placement and routing program. The last evolution involves a detailed Boolean description of leaf cells followed by a transistor level implementation of leaf cells and mask generation. In the standard based design style, leaf cells are pre-designed (at the transistor level) and stored in a library for logic implementation, effectively eliminating the need for the transistor level design.

Q-5-a) Draw CPL NAND gate circuit only.

ANS



Q-5-b) Distinguish static logic with Dynamic logic

ANS

Static CMOS is a logic circuit design technique whereby the output is always strongly driven due to it always being connected to either VCC or GND (except when switching). A static CMOS circuit is composed of two networks:

- pull-up network (PUN) - a set of PMOS transistors connected between V_{cc} and the output line
- pull-down network (PDN) - a set of NMOS transistors connected between GND and the output line

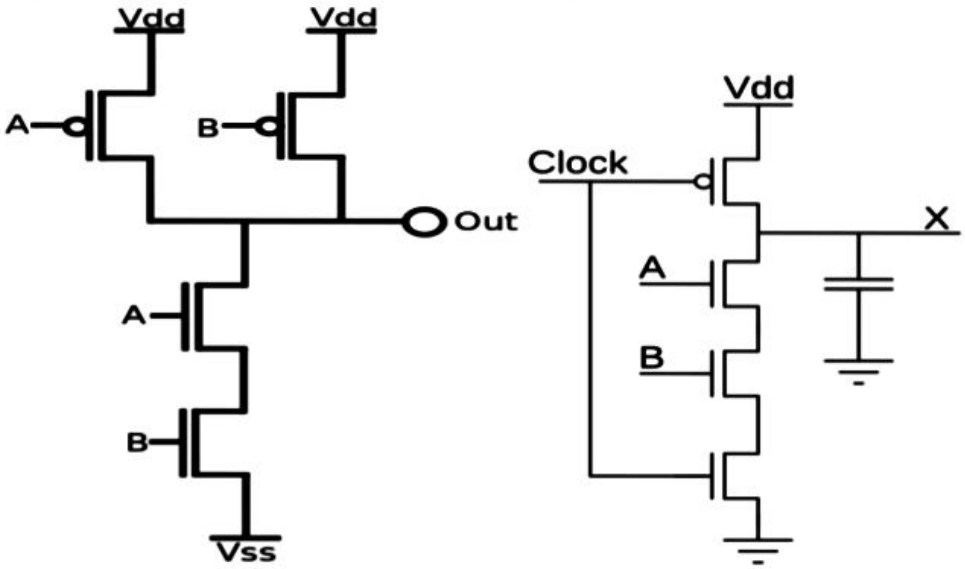
Components designed out pull-up and pull-down networks operate in a mutually exclusive way; in a steady state there is never a direct path between Vcc and GND. Devices that are made up of PUN/PDN are always strongly driven and therefore offers strong immunity from noise. When both the pull-up and pull-down networks are OFF, the result is high impedance. That state is important for memory elements, tristate bus drives, and various other components such as some multiplexers and buffers. When both the pull-up and pull-down networks are ON, the result is a crowbarred level. This result is typically an unwanted condition.

Static logic is slower because it has twice the capacitive loading, higher thresholds, and uses slow P transistors for **logic**. In general, **dynamic logic** greatly increases the number of transistors that are switching at any given

time, which increases power consumption over **static CMOS**. **Dynamic logic** (or sometimes **clocked logic**) is a design methodology in combinatory logic circuits, particularly those implemented in MOS technology. Dynamic logic is distinguished from so-called *static logic* in that dynamics logic uses a clock signal in its implementation of combinational logic circuits. The usual use of a clock signal is to synchronize transitions in sequential logic circuits. Dynamic logic requires a minimum clock rate fast enough that the output state of each dynamic gate is used or refreshed before the charge in the output capacitance leaks out enough to cause the digital state of the output to change, during the part of the clock cycle that the output is not being actively driven.

Static logic has no minimum clock rate—the clock can be paused indefinitely. While it may seem that doing nothing for long periods of time is not particularly useful, it leads to two advantages:

- being able to pause a system at any time makes debugging and testing much easier, enabling techniques such as single stepping.
- being able to run a system at extremely low clock rates allows low-power electronics to run longer on a given battery.



Ex- Static CMOS Logic:
This ckt. Implements the logic function, Out = $\overline{AB}$

If A and B are both high, the output will be pulled low and if both A and B are low, the output will be high.

Ex- Dynamic CMOS Logic:
This ckt. Implements the same logic function,

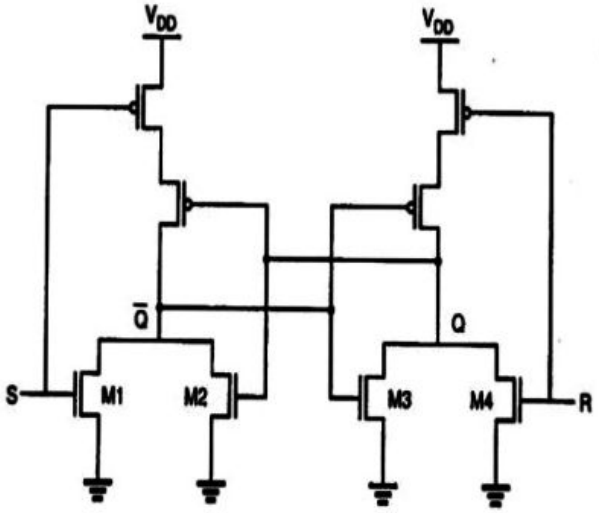
The dynamic logic circuit requires two phases. The first phase, when *Clock* is low, is called the *setup phase* or the *precharge phase* and the second phase, when *Clock* is high, is called the *evaluation phase*. In the setup phase, the output is driven high unconditionally (no matter the values of the inputs *A* and *B*). The capacitor, which represents the load capacitance of this gate, becomes charged. Because the transistor at the bottom is turned off, it is impossible for the output to be driven low during this phase.

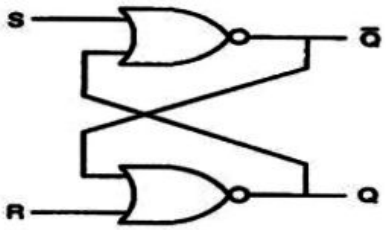
During the *evaluation phase*, *Clock* is high.
If *A* and *B* are also high, the output will be pulled low. Otherwise, the output stays high (due to the load

Q-5-c) Design and describe SR Latch with neat circuit diagram.

ANS:-

The Bistable element consisting of two cross-coupled inverters has two stable operating modes or states. The ckt.preserves it any one state as long as the power supply voltage is provided, hence, the ckt.can perform a simple memory function of holding its state. However, the simple two-inverter ckt.examined above has no provision for allowing its state to be changed externally from one stable operating mode to the other. To allow such a change of state, we must add simple switches to the bistable element, which can be used to force or trigger the ckt.from one operating point to the other. Below figure shows a simple CMOS SR latch which has two such triggering inputs, S (set) and R (reset). It is also called SR flip-flop since two stable states can be switched back and forth. The ckt.consists of two CMOS NOR2 gates. One of the input terminals of each NOR gate is used to neither cross couple to the output of the other NOR gate, while the second input enables triggering of the ckt.





S	R	Q_{n+1}	$\bar{Q}_{n+1}$	Operation
0	0	Q_n	$\bar{Q}_n$	hold
1	0	1	0	set
0	1	0	1	reset
1	1	0	0	not allowed

Q-6-a) What is noise Margins?

ANS

Noise margin (NM) is the amount of noise that a CMOS circuit could withstand without compromising the operation of circuit. Noise margin does make sure that any signal which is logic '1' with finite noise added to it, is still recognized as logic '1' and not logic '0'.

$NM_L = V_{IL} - V_{OL}$

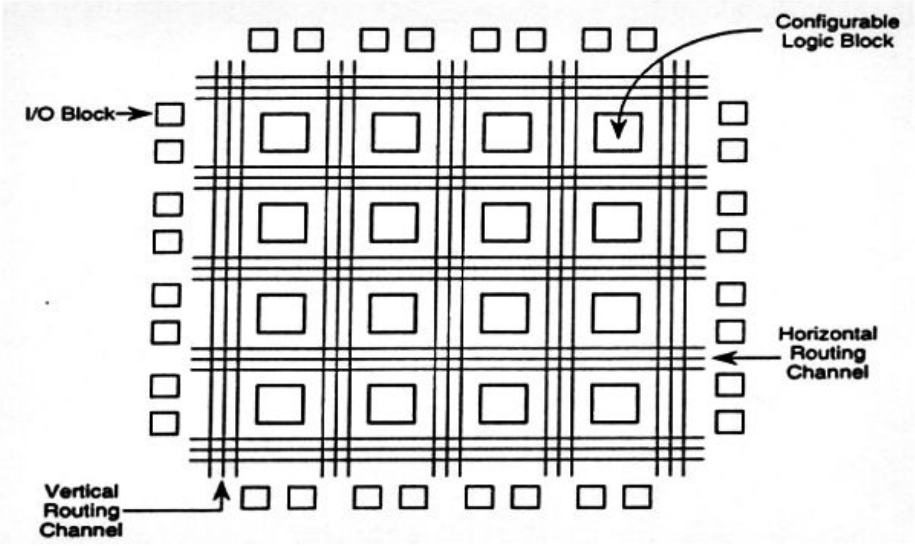
$NM_H = V_{OH} - V_{IH}$

Q-6-b) Describe design strategy by FPGA.

ANS

FPGA design style provides a means for fast prototyping and also for cost effective chip design, especially for low volume application. The full form of **FPGA** is **"Field Programmable Gate Array"**. It contains ten thousand to more than a million logic gates with programmable interconnection. Programmable interconnections are available for users or designers to perform given functions easily. A typical model FPGA chip is shown in the given figure. There are I/O

blocks, which are designed and numbered according to function. For each module of logic level composition, there are **CLB's (Configurable Logic Blocks)**.



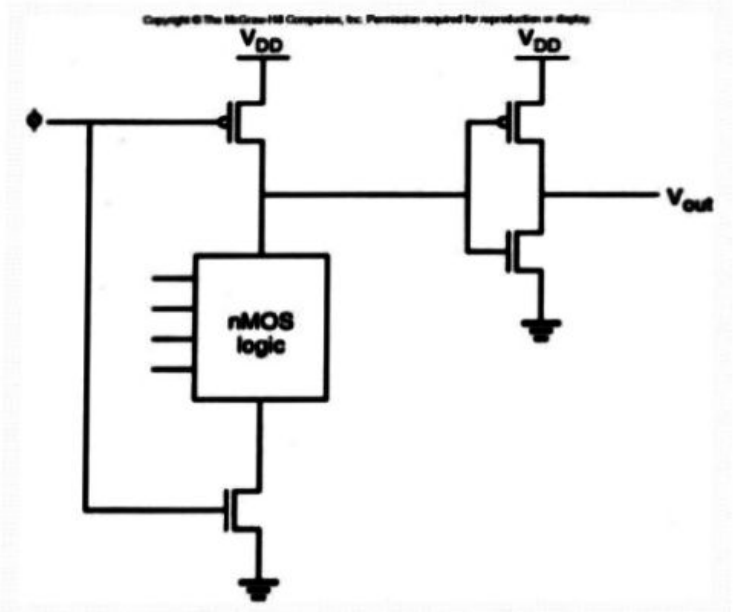
CLB performs the logic operation given to the module. The inter connection between CLB and I/O blocks are made with the help of horizontal routing channels, vertical routing channels and PSM (Programmable Multiplexers).

The number of CLB it contains only decides the complexity of FPGA. The functionality of CLB's and PSM are designed by VHDL or any other hardware descriptive language. After programming, CLB and PSM are placed on chip and connected with each other with routing channels.

Q-6-c) Describe cascaded domino CMOS logic gate with neat circuit diagram.

ANS

Consider the generalized ckt. diagram of a domino CMOS logic gate shown the figure. A dynamic CMOS logic state, is cascaded with static CMOS inverter stage. The addition of the inverter allows us to operate a number of such structures in cascade, is explained in the following –



During the pre-charge phase (when CK = 0), the output node of the dynamic CMOS stage is pre-charged to a high logic level, and the out of the CMOS inverter (buffer) becomes low. When the clock signal rises at the beginning of the evaluation phase, there are two possibilities. The output node of the dynamic CMOS stage is either discharged to a low level through the nMOS circuitry (1 to 0 transitions) or it remains high.

Consequently, the inverter output voltage can also make at most one transition during the evaluation phase, from 0 to 1. Regardless of the input voltage applied to the dynamic CMOS stage, it is not possible for the buffer output to make a 1 to 0 transition during the evaluation phase.

********** END **********