PNS SCHOOL OF ENGINEERING & TECHNOLOGY

MASHAGHAI,KENDRAPRARA

DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION

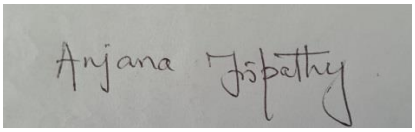
LESSON PLAN

BY MRS.ANJANA TRIPATHY

ON VLSI LAB(PRACTICAL-02)

MONTH	WEEK	DATE	NAME OF THE EXPERIMENT
SEPTEMBER	3RD	15/09/2022	1. Develop a VHDL test bench code for testing following and implement on FPGA kit a. Addition b. Subtraction c. Multiplication d. Division.
	4TH	22/09/2022	2. Develop a VHDL test bench code for testing following and implement on FPGA kit
	5TH	29/09/2022	3. Develop a VHDL test bench code for testing 4 x 4 matrix keypad interface. a. Write a VHDL Code forRelay interface b. Buzzer Interface
OCTOBER	2ND	13/10/2022	4. Develop a VHDL test bench code for testing 7 segment LED display interface. 5. Develop a VHDL test bench code for testing Stepper motor interface.
	3RD	20/10/2022	6. Develop a VHDL test bench code for testing Traffic light control.
	4TH	27/10/2022	7. Develop a VHDL test bench code for testing 4 bit binary counter and study all using simulation software.
NOVEMBER	1ST	3/11/2022	9. Develop a VHDL test bench code for testing any one of the simple gate Simulate the test bench code in the HDL software.
	2ND	10/11/2022	10. Develop a VHDL test bench code for testing for generator PW M signals for DC Motor control.
	3RD	17/11/2022	11. Develop a VHDL test bench code & implement of FPGA kit for MUX & DEMUX.
	1ST	1/11/2022	12. Develop a VHDL test bench code & implement of FPGA kit for Encoder, Decoder & Shift Register.

DECEMBER	2ND	8/12/2022	6. Develop a VHDL test bench code for testing Traffic light control.
	3RD	15/12/2022	14. Development of small Project using Verilog i.e. Generate music using PC Hardware.
	4TH	22/12/2022	RECORD DEPOSITE/VIVA



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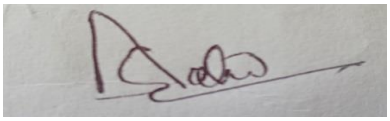

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