PNS SCHOOL OF ENGG. & TECH., MARSHAGHAI
DEPARTMENT OF ELECTRONICS & TELECOMMUNICATION ENGINEERING

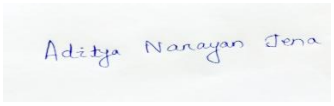
LESSON PLAN

BRANCH : ETC & COMP. SC ENGINEERING	SEMESTER : 4TH	NAME OF TEACHING FACULTY : **ER. ADITYA NARAYAN JENA**
SUBJECT : Microprocessor & Microcontroller	**NO. OF DAYS/ PER WEEK CLASS ALLOTTED : 05**	**SEMESTER FROM DATE : 14.02.2023 TO 23.05.2023** **NO. OF WEEKS : 15**

WEEK	CLASSDAY	THEORY TOPICS
1ST	1st	**1.8085 microprocessor** Discussion of microprocessor and its application
	2nd	Distinguish between microprocessor and microcomputer
	3rd	Discussion of Bus system in processor
	4th	Pin configuration of Intel 8085 microprocessor
	5th	Revision
2ND	1st	Pin configuration of Intel 8085 microprocessor
	2nd	Pin configuration of Intel 8085 microprocessor
	3rd	Architecture of Intel 8085 processor
	4th	Architecture of Intel 8085 processor
	5th	Revision
3RD	1st	Registers of Intel 8085. Distinguish between SPR and GPR
	2nd	Stack, stack pointer and stack top
	3rd	8085 interrupts
	4th	**2.Instruction set and A** Addressing modes in Intel 8085
	5th	Revision
4TH	1st	Types of instruction
	2nd	Simple programming examples
	3rd	Basic assembler Directives
	4th	Programming on logic operations
	5th	Revision
5TH	1st	Programming on logic operations
	2nd	Programming on Counter
	3rd	Programming on Delay

	4th	Programming on looping, counting , Indexing(JMP and CALL)
	5th	Revision
6TH	1st	Compare between two numbers, Arrray Handling, code conversion
	2nd	Memory & I/O addressing
	3rd	**3.Timing diagram** T-state, Fetch cycle, Machine cycle and Instruction cycle
	4th	Differentiate between Instruction cycle, machine cycle and T state
	5th	Revision
7TH	1st	Timing diagram of memory read, memory write, opcode fetch machine cycle.
	2nd	Timing diagram of I/O read & I/O write machine cycle.
	3rd	Timing diagram of MOV, MVI .
	4th	Timing diagram of LDA.
	5th	Revision
8TH	1st	**4. Microprocessor based system development Aids.** Concept of Interfacing .
	2nd	Memory mapping and I/O mapping.
	3rd	Pin configuration of Intel 8255 .
	4th	Memory interfacing with RAM and EPROM .
	5th	Revision
9TH	1st	ADC and DAC interfacing
	2nd	Traffic light controlling, stepper motor control, 7 segment display.
	3rd	Concept of DMA controller, USART.
	4th	**5.8086 Microprocessor** Registers in 8086.
	5th	Revision
10TH	1st	Internal architecture of Intel 8086, maximum and minimum mode .
	2nd	Internal architecture of Intel 8086, maximum and minimum mode .
	3rd	Internal architecture of Intel 8086, maximum and minimum mode .
	4th	Class test .
	5th	Revision
11TH	1st	Pin details of 8086.
	2nd	Pin details of 8086 .
	3rd	Pin details of 8086 .

	4th	Addressing modes of 8086
	5th	Revision
12TH	1st	Interrupts in 8086.
	2nd	Instruction set of 8086.
	3rd	Simple programming in8086.
	4th	Simple programming in 8086.
	5th	Revision
13TH	1st	**6. Microcontroller** Distinguish between Microprocessor & Microcontroller .
	2nd	8 bit & 16 bit microcontroller
	3rd	CISC & RISC processor.
	4th	Architecture of 8051 Microcontroller.
	5th	Revision
14TH	1st	Signal Description of 8051 Microcontrollers
	2nd	Memory Organisation-RAM structure, SFR
	3rd	Registers,timers,interrupts of 8051 Microcontrollers
	4th	Addressing modes of 8051
	5th	Revision
15TH	1st	Simple 8051 Assembly Language Programming Arithmetic& Logic Instructions , JUMP, LOOP, CALL Instructions, I/O Port Programming
	2nd	Interrupts, Timer & Counters , Serial Communication
	3rd	Microcontroller interrupts and interfacing with 8255
	4th	Final revision, previous year questions discussion.
	5th	Final Revision



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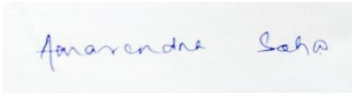

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