PNS SCHOOL OF ENGG. & TECH., MARSHAGHAI

DEPARTMENT OF ELECTRONICS & TELECOMMUNICATION ENGINEERING

LESSON PLAN

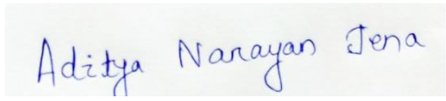
BRANCH : **ETC ENGINEERING**	**SEMESTER :** **5TH**	**NAME OF THE TEACHING FACULTY :** **MR. ADITYA NARAYAN JENA**
SUBJECT : **VLSI & EMBEDDED SYSTEM**	**NO. OF DAYS PER WEEK CLASS ALLOTTED :** **05**	**SEMESTER FROM DATE: 01.08.2023 TO 30.11.2023**

WEEK	**CLASSDAY**	**THEORY TOPICS**
1ST	1st	**1.INTRODUCTION TO VLSI AND MOS TRANSISTOR** HISTORICAL PERSPECTIVE-INTRODUCTION,CLASSIFICATION OF CMOS DIGITAL
	2nd	INTRODUCTION TO MOS TRANSISTOR AND BASIC OPERATION OF MOSFET
	3rd	STRUCTURE AND OPERATION OF NMOS ENHANCEMENT TYPE MOSFET
	4th	STRUCTURE AND OPERATION OF CMO
	5th	MOSFET VI CHARACTERSTICS
2ND	1st	WORKING OF MOSFET CAPACITANCES
	2nd	MODELLING OF MOS TRANSISTORS,CONCEPT OF SPICE LEVEL-1 MODELS,LEVEL-2 MODELS,LEVEL-3 MODEL
	3rd	DESIGN FLOW CIRCUIT PROCEDURES
	4th	VLSI DESIGN FLOW
	5th	Y-CHART
3RD	1st	DESIGN HIERARCHY
	2nd	VLSI DESIGN STYLES-FPGA,GATE ARRAY DESIGN
	3rd	STANDARD CELL BASED DESIGN STYLE,FULL CUSTOM DESIGN STYLE
	4th	**2.FABRICATION OF MOSFET** SIMPLIFIED PROCESS SEQUENCE FOR FABRICATION
	5th	BASIC STEPS IN FABRICATION PROCESS FLOW
4TH	1st	FABRICATION PROCESS OF NMOS TRANSISTOR
	2nd	FABRICATION PROCESS OF NMOS TRANSISTOR
	3rd	CMOS N-WELL FABRICATION PROCESS FLOW
	4th	CMOS N-WELL FABRICATION PROCESS FLOW
	5th	MOS FABRICATION PROCESS BY N-WELL ON P-SUBTRATE
5TH	1st	REVISION
	2nd	CMOS FABRICATION PROCESS BY P-WELL ON N-SUBTRATE
	3rd	LAYOUT DESIGN RULES

	4th	STICK DIAGRAMS OF CMOS INVERTER
	5th	**3.MOS INVERTER** BASIC NMOS INVERTERS
6TH	1st	WORKING OF RESISTIVE-LOAD INVERTER
	2nd	INVERTER WITH N-TYPE MOSFET LOAD-ENHANCEMENT LOAD
	3rd	DEPLETION NMOS INVERTER
	4th	CIRCUIT OPERATION OF CMOS INVERTER
	5th	CHARACTERSTICS AND INTERCONNECT EFFECTS OF CMOS INVERTER,DELAY TIME DEFINATIONS
7TH	1st	CMOS INVERTER DESIGN WITH DELAY CONSTRAINTS-TWO SAMPLE MASK LAY OUT FOR P-TYPE SUBTRATE
	2nd	**4.STATIC COMBINATIONAL,S EQUENTIAL,DYANA MICS LOGIC CIRCUITS AND MEMORIES** DEFINE STATIC COMBINATIONAL LOGIC,WORKING OF STATIC CMOS LOGIC CIRCUITS(TWO-INPUT NAND GATE)
	3rd	CMOS LOGIC CIRCUITS(NAND2 GATE)
	4th	CMOS TRANSMISSION GATES(PASS GATE)
	5th	BASICS OF COMPLEX LOGIC CIRCUITS,CLASSIFICATION OF LOGIC CIRCUITS BASED ON THEIR TEMPORAL BEHAVIOUR
8TH	1st	SR FLIP LATCH CIRCUIT,CLOCKED SR LATCH WORKING
	2nd	CMOS D LATCH OPERATION
	3rd	INTRODUCTION TO MICROPROCESSOR AND
	4th	BASIC PRINCIPLES OF DYANAMIC PASS TRANSISTOR CIRCUITS;DYNAMIC RAM,SRAM
	5th	OPERATION OF FLASH MEMORY
9TH	1st	REVISION
	2nd	**5.SYSTEM DESIGN METHOD AND SYNTHESIS** DESIGN LANGUAGE(SPL AND HDL) AND EDA TOOLS
	3rd	VHDL AND PACKAGE XLINX
	4th	DESIGN STRATEGIES AND CONCEPT OF FPGA WITH STANDARD CELL BASED DESIGN
	5th	VHDL FOR DESIGN SYNTHESIS USING CPLD OR FPGA
10TH	1st	BASIC IDEA OF RASPBERRY PI
	2nd	**6.INTRODUCTION TO EMBEDDED SYSTEMS** OVERVIEW OF EMBEDDED SYSTEMS,LIST OF EMBEDDED SYSTEMS
	3rd	CHARACTERSTICS OF EMBEDDED SYSTEMS

	4th	DIGIAL CAMERA-COMPONENTS AND OPERATION
	5th	EMBEDDED SYSTEM TECHNOLOGIES-TECHNOLOGY FOR EMBEDDED SYSTEMS
11TH	1st	PROCESSOR TECHNOLOGY,IC TECHNOLOGY
	2nd	DESIGN TECHNOLOGY-PROCESSOR TECHNOLOGY
	3rd	GENERAL PURPOSE PROCESSORS-SOFTWARE
	4th	BASIC ARCHITECTURE OF SINGLE PURPOSE PROCESSORS-HARDWARE
	5th	APPLICATION-SPECIFIC PROCESSORS,MICROCONTROLLERS,DIGITAL SIGNAL PROCESSORS(DSP)
12TH	1st	IC TECHNOLOGY-FULL CUSTOM/VLSI
	2nd	SEMI CUSTOM ASIC(GATE ARRAY AND STANDARD CELL)
	3rd	OPERATION OF PROGRAMMABLE LOGIC DEVICE(PLD)
	4th	BASIC IDEA OF ARDUINO MICROCONTROLLER
	5th	REVISION

SIGNATURE OF H.O.D



SIGNATURE OF LECTURER