PNS SCHOOL OF ENGG. & TECH., MARSHAGHAI

DEPARTMENT OF ELECTRICAL ENGINEERING

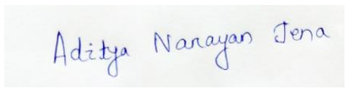
LESSON PLAN

BRANCH : ELECTRICAL ENGINEERING	**SEMESTER : 5TH**	**NAME OF THE TEACHING FACULTY :** **MR. ADITYA NARAYAN JENA**
SUBJECT : DIGITAL ELECTRONICS & MICROPROCESSOR	**NO. OF DAYS PER WEEK CLASS ALLOTTED : 05**	**SEMESTER FROM DATE: 01.08.2023 TO 30.11.2023**
WEEK	**CLASSDAY**	**THEORY TOPICS**
1ST	1st	**1.BASIC OF DIGITAL ELECTRONOICS** INTRODUCTION TO DIGITAL ELECTRONICS
	2nd	NUMBER SYSTEM(BINARY,OCTAL,DECIMAL,HEXADECIMAL)
	3rd	CONVERSION OF BINARY/OCTAL/HEXADECIMAL NUMBER SYSTEM INTO DECIMAL NUMBER SYSTEM
	4th	CONVERSION OF DECIMAL NUMBER SYSTEM INTO BINARY/OCTAL/HEXADECIMAL NUMBER SYSTEM
	5th	CONVERSION OF BINARY TO OCTAL AND OCTAL TO BINARY,BINARY TO HEXADECIMAL AND HEXADECIMAL TO BINARY NUMBER SYSTEM,CONVERSION OF OCTAL INTO HEXADECIMAL AND HEXADECIMAL INTO OCTAL NUMBER SYSTEM
2ND	1st	BINARY ARITHMATIC (ADDITION,SUBTRACTION,MULTIPLICATION,DIVISION)
	2nd	1'S COMPLEMENT AND 2'S COMPLEMENT METHOD,SUBTRACTION USING 2'S COMPLEMENT METHOD
	3rd	BINARY CODES(BCD CODE,XS-3 CODE,GRAY CODE)
	4th	LOGIC GATES(AND,OR,NOT,NAND,NOR,XOR,XNOR) AND TRUTH TABLE
	5th	UNIVERSAL GATE AND IMPLEMENTATION USING NAND AND NOR GATES
3RD	1st	DEMORGANS THEOREM AND ITS PROOF
	2nd	BOOLEAN ALGEBRA,SIMPLIFICATION OF LOGIC EXPRESSION USING BOOLEAN ALGEBRA
	3rd	BOOLEAN EXPRESSION(SOP,POS)
	4th	2-VARIABLE,3-VARIABLE,4-VARIABLE K-MAP
	5th	SIMPLIFICATION OF SOP AND POS EXPRESSION USING K-MAP
4TH	1st	DON'T CARE CONDITION
	2nd	**2.COMBINATIONAL LOGIC CIRCUIT** CONCEPT OF COMBINATIONAL LOGIC CIRCUIT, HALF ADDER CIRCUIT,WORKING
	3rd	HALF ADDER USING NAND GATES ONLY AND NOR GATES ONLY,FULL ADDER WORKING,LOGIC DIAGRAM
	4th	REALIZE FULL ADDER USING TWO HALF-ADDERS AND AN OR-GATE WITH TRUTH TABLE,HALF SUBTRACTOR WORKING AND ITS LOGIC DIGRAM

	5th	FULL SUBSTRACTOR WORKING,LOGIC DIAGRAM
5TH	1st	REVISION
	2nd	2:4 DECODER,3:8 DECODER WORKING,LOGIC DIAGRAM
	3rd	4:2 ENCODER,OCTAL TO BINARY ENCODER WORKING,BINARY-DECIMAL ENCODER WORKING,LOGIC DIAGRAM
	4th	MUX,4:1 MUX WORKING,LOGIC DIAGRAM
	5th	**3.SEQUENTIAL LOGIC CIRCUIT** DMUX,1:4 DMUX WORKING,LOGIC DIAGRAM
6TH	1st	1-BIT COMPARATOR AND 2-BIT COMPARATOR WORKING,TRUTH TABLE,LOGIC DIAGRAM
	2nd	SLC,TYPES OF SLC, DIFFERENCE BETWEEN CLC AND SLC,CONCEPT OF CLOCK AND TRIGGERING
	3rd	FLIP-FLOPS,NOR BASED SR-FF TRUTH TABLE AND WORKING
	4th	NAND BASED SR-FF WORKING,CLOCKED NAND BASED SR-FF WORKING
	5th	WORKING OF CLOCKED D-FF AND JK-FF
7TH	1st	RACE-AROUND CONDITION,WORKING OF MASTER-SLAVE JK-FF
	2nd	WORKING OF T FLIP-FLOP,APPLICATIONS OF FLIP-FLOPS
	3rd	COUNTERS, TYPES OF COUNTERS,DIFFERENCE BETWEEN ASYNCHRONOUS AND SYNCHRONOUS COUNTER,MODULUS OF A COUNTER
	4th	4-BIT ASYNCHRONOUS COUNTER,TIMING DIAGRAM
	5th	REGISTERS AND ITS TYPES,WORKING OF SISO REGISTER
8TH	1st	WORKING OF SIPO AND PISO REGISTER
	2nd	WORKING OF PIPO REGISTER
	3rd	INTRODUCTION TO MICROPROCESSOR AND MICROCOMPUTER
	4th	PIN DIAGRAM AND DESCRIPTION OF 8085 MICROPROCESSOR
	5th	PIN DESCRIPTION OF 8085 MICROPROCESSOR
9TH	1st	REVISION
	2nd	BLOCK DIAGRAM/ARCHITECTURE OF 8085 MICROPROCESSOR
	3rd	ARCHITECTURE OF 8085
	4th	REGISTERS OF 8085,STACK,STACK POINTER,STACK TOP
	5th	**4.8085 MICROPROCESSOR** OPCODES, OPERANDS, INSTRUCTION TYPES ACCORDING TO BYTE SIZE(1-BYTE,2-BYTE,3-BYTE INSTRUCTIONS WITH EXAMPLES
10TH	1st	INSTRUCTION SET TYPES ACCORDING TO OPERATION PERFORMED BY MICROPROCESSOR(DATA TRANSFER,ARITHMATIC,LOGICAL,BRANCH,STACK,MACHINE CONTROL,I/O CONTROL)
	2nd	ADDRESSING MODES OF 8085 MICROPROCESSOR

	3rd	INSTRUCTION CYCLE, FETCH CYCLE,EXECUTION CYCLE,MACHINE CYCLE AND T-STATE
	4th	TIMING DIAGRAM OF OPCODE FETCH CYCLE, MEMORY READ AND MEMORY WRITE CYCLE
	5th	TIMING DIAGRAM OF I/O READ,I/O WRITE,MOV, MVI INSTRUCTION
11TH	1st	COUNTER AND TIME DELAY
	2nd	SIMPLE ASSEMBLY LANGUAGE PROGRAMMING OF 8085 MICROPROCESSOR
	3rd	**5.INTERFACING & SUPPORT CHIPS** BASIC CONCEPT OF INTERFACING, MEMORY MAPPING AND I/O MAPPING
	4th	8255PPI PIN DESCRIPTION
	5th	8255PPI FUNCTIONAL BLOCK DIAGRAM
12TH	1st	MODES OF 8255
	2nd	APPLICATION USING 8255 PPI-SEVEN SEGMENT LED DISPLAY
	3rd	SQUARE WAVE GENERATOR
	4th	TRAFFIC LIGHT CONTROLLER
	5th	REVISION

SIGNATURE OF H.O.D



SIGNATURE OF LECTURER