

PNS SCHOOL OF ENGINEERING AND TECHNOLOGY, MARSHAGHAI, KENDRAPARA
LESSION PLAN

| Branch: ETC & COMPUTER SC. Subject: Pr-3 Digital Electronics Lab. | Sem-3rd No.of days per week: 2 Class Allotted: 60 | <p align="center"> Name of the teaching faculty: Anjana Tripathy Semestar From Date :01.08.2023 to 30.11.2023 No. of weeks : 14 </p> |
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| MONTH | WEEK | PRATICAL TOPIC |
| September | 1st | Familiarization of Digital Trainer Kit, Logic Pulser Light probes & Digital Ics, IE-7400, 7402, 7404, 7408, 7432 & 7486 (Draw Pin Diagrams) |
| | 2nd | Verify truth table of AND, OR, NOT, NOR, NAND, & OR, X-NOR gates |
| | 3rd | Impliment various gates by using universal of NAND & NOR Gates Impliment various gates by using universal of NAND & NOR Gates |
| October | 4th | Impliment various gates by using universal of NAND & NOR Gates |
| | 5th | Impliment half adder and full adder using logic gates |
| | | Construct & verify operation of full adder using logic gates. |
| | 6th | Construct & verify operation of half subtractor using logic gates. |
| | | Construct & verify operation of full subtractor using logic gates. |
| November | 7th | Design & Implement a 4-bit Binary to gray Code Converter. |
| | | Design & Implement a 4-bit Binary to gray Code Converter. |
| | 8th | Design & Implement a single bit Digital Comparator Circuit. |
| | | Design & Implement a two bit Digital Comparator Circuit. |
| | 9th | Design Multiplexer (4 : 1) |
| | | Design De-Multiplexer (1 : 4) |
| 10th | Study the operation of Flip-Flop, S.R Flip Flop | |
| | Study the operation of J.K. Flip Flop | |
| December | 11th | Study the operation of D Flip Flop, T Flip Flop |
| | | Realize a 4-bit a synachronous up/down counter with a control for up/dow counting. |
| | 12th | Realize a 4-bit a synachronous up/down counter with a control for up/dow counting. |
| | | Study Shift Registers |
| | 13th | Verify the operation 8-bit D/A and A/D Conversion & Test. |
| 14th | Verify the operation 8-bit D/A and A/D Conversion & Test. | |

Sign of Lecturer

Sign of HOD