PNS SCHOOL OF ENGINEERING AND TECHNOLOGY		
Branch: Electrical Engg.	Semester: 5th	Name of the Demonstrator: **Anjana Tripathy.**
Subject: DEM Lab	No of Classes Alloted in a Week: 2	Duration of Semester: 01.08.2023 - 30.11.2023
Week	Class Day	Theory / practical Topic
1st	1	Verify truth tables of AND, OR, NOT, NOR, NAND, XOR, XNOR gates
	2	Verify truth tables of AND, OR, NOT, NOR, NAND, XOR, XNOR gates
2nd	1	Verify truth tables of AND, OR, NOT, NOR, NAND, XOR, XNOR gates
	2	Implement various gates by using universal properties of AND & NOR gates and verify truth table
3rd	1	Implement various gates by using universal properties of AND & NOR gates and verify truth table
	2	Implement half adder and Full adder using logic gates
4th	1	Implement half adder and Full adder using logic gates
	2	Implement half subtractor and Full subtractor using logic gates
5th	1	Implement half subtractor and Full subtractor using logic gates
	2	Implement a 4-bit Binary to Gray code converter
6th	1	Implement a Single bit digital comparator
	2	Study Multiplexer
7th	1	Study demultiplexer
	2	Study of flip-flops i) S-R flip flop ii) J-K flip flop iii) flip flop iv) T flip flop
8th	1	Study of flip-flops i) S-R flip flop ii) J-K flip flop iii) flip flop iv) T flip flop
	2	Realize a 4-bit asynchronous UP/Down counter with a control for up/down counting
9th	1	Realize a 4-bit synchronous UP/Down counter with a control for up/down counting
	2	Implement Mode-10 asynchronous counters
10th	1	Study shift registers
	2	1'S Complement
11th	1	2'S Complement
	2	Addition of 8-bit number
12th	1	Subtraction of 8-bit number resulting 8/16 bit number
	2	Decimal Addition 8-bit number
13th	1	Decimal Subtraction 8-bit number
	2	Compare between two numbers & Find the largest in an Array
14th	1	Block Transfer
	2	Traffic light control using 8255

Signature of the Demonstrator

Signature of the H.O.D.