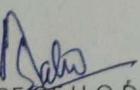
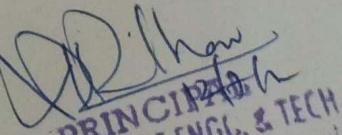


PNS SCHOOL OF ENGINEERING AND TECHNOLOGY, MARSHAGHAI, KENDRAPARA
LESSON PLAN

Branch: ETC Engineering. Subject: Pr-3 Digital Electronics Lab.	Sem-3rd No.of days per Class Allotted	Name of the teaching faculty: Anjana Tripathy Semestar From Date :14.07.2025 to 15.11.2025 No. of weeks : 14
MONTH	WEEK	PRACTICAL TOPIC
July	1st	Familiarization of Digital Trainer Kit, Logic Pulser Light probes & Digital Ics, IE-7400, 7402, 7404, 7408, 7432 & 7486 (Draw Pin Diagrams)
	2nd	Verify truth table of AND, OR, NOT, NOR, NAND, & OR, X-NOR gates
	3rd	Impliment verious gates by using universal of NAND & NOR Gates
	3rd	Impliment verious gates by using universal of NAND & NOR Gates
August	4th	Impliment verious gates by using universal of NAND & NOR Gates
	5th	Impliment half adder and full adder using logic gates
	5th	Construct & verify operation of full adder using logic gates.
	6th	Construct & verify operation of half subtractor using logic gates.
	6th	Construct & verify operation of full subtractor using logic gates.
	7th	Design & Implement a 4-bit Binary to gray Code Converter.
September	7th	Design & Implement a 4-bit Binary to gray Code Converter.
	8th	Design & Implement a single bit Digital Comparator Circuit.
	8th	Design & Implement a two bit Digital Comparator Circuit.
	9th	Design Multiplexer (4 : 1)
	9th	Design De-Multiplexer (1 : 4)
October	10th	Study the operation of Flip-Flop, S.R Flip Flop
	10th	Study the operation of J.K. Flip Flop
	11th	Study the operation of D Flip Flop, T Flip Flop
	11th	Realize a 4-bit a synchronous up/down counter with a control for up/dow counting.
November	11th	Realize a 4-bit a synchronous up/down counter with a control for up/dow counting.
	12th	Study Shift Registers
	13th	Verify the operation 8-bit D/A and A/D Conversion & Test.
	14th	Verify the operation 8-bit D/A and A/D Conversion & Test.


 SIGNATURE OF H.O.D.


 SIGNATURE OF DEMONSTRATOR


 PRINCIPAL
 PNS SCHOOL OF ENGG. & TECH
 Nishamani Vihar, Marshaghai