PNS SCHOOL OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS & TELECOMMUNICATION ENGINEERING

Branch: ETC Engg.	Semester: 3rd	Name of the Lecturer: **Aditya Narayan Jena**
Subject: DEC	Classes Alloted in a Week: 4	Duration of Semester: 14.07.2025 - 15.11.2025
Week	Class Day	Theory / Practical Topic
1st	1	**LOGIC GATES:** OR,AND,NOT gates
	2	NAND,NOR,XOR,XNOR Gates
	3	Integrated circuits
	4	Fan In,Fan out,Termination of unused inputs
2nd	1	AND and OR From NAND & NOR gates
	2	**BOOLEAN ALGEBRA:** Boolean Operations(OR,AND,NOT)
	3	Representation of logic circuits by Boolean expression
	4	Laws of Boolean Algebra
3rd	1	DeMorgans theorem
	2	Logic circuit simplification
	3	Equivalent logic gates
	4	NAND & NOR Implementions of logic circuits
4th	1	SOP
	2	POS
	3	K-Map
	4	K-Map
5th	1	K-Map
	2	**COMBINATIONAL LOGIC CIRCUITS:** Half Adder
	3	Full Adder
	4	Half Subtractor,Full Subtractor
6th	1	4-bit Adder
	2	MUX,DMUX
	3	Decoder,Encoder
	4	Digital Comparator
7th	1	7-Segement Decoder
	2	**LATCHES & FLIP-FLOPS:** NOR Latch
	3	NAND Latch
	4	Gated SR Latch
8th	1	Gated D Latch
	2	Master Slave JK-FF
	3	SR-FF,D-FF
	4	JK-FF,T-FF,Timing diagram
9th	1	**COUNTERS:** Binary counters
	2	Up-down counter
	3	Asynchronous counter
	4	Synchronous counter

10th	1	Decade counter
	2	MOD-N Counter
	3	Divide by N counter
	4	Synchronous counter using D-FF,JK-FF
11th	1	**SHIFT REGISTERS:** SISO,SIPO register
	2	PIPO,PISO register
	3	Ring counter
	4	Self starting Ring counter
12th	1	Johnson counter
	2	**SEMICONDUCTOR MEMORIES:** Define RAM,ROM,PROM,EPROM
	3	Memory cell
	4	Small Diode Matrix ROM
13th	1	Dynamic Memory
	2	Dynamic vs Static memory
	3	Advantages and Disadvantages of Dynamic and Static Memory
	4	**SEQUENTIAL CIRCUIT DESIGN:** Combiantional vs Sequential circuits
14th	1	Adder,Subtractor
	2	Decoder
	3	MUX,DMUX
	4	Comparator, Concept of Finite state machines

Signature of the Lecturer **Signature of the H.O.D.** **Signature of the Principal**