PNS SCHOOL OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ETC ENGINEERING

Branch: ETC Engg.	Semester: 5TH	Name of the Lecturer: **Aditya Narayan Jena**
Subject: VLSI & ES	Classes Alloted in a Week: 4	Duration of Semester: 14.07.2025 - 15.11.2025
Week	Class Day	Theory / Practical Topic
1st	1	**1.INTRODUCTION TO VLSI AND MOS TRANSISTOR**
	2	INTRODUCTION TO MOS TRANSISTOR AND BASIC OPERATION OF MOSFET
	3	STRUCTURE AND OPERATION OF NMOS ENHANCEMENT TYPE MOSFET
	4	STRUCTURE AND OPERATION OF CMO
2nd	1	MOSFET VI CHARACTERSTICS
	2	WORKING OF MOSFET CAPACITANCES
	3	MODELLING OF MOS TRANSISTORS,CONCEPT OF SPICE LEVEL-1 MODELS,LEVEL-2 MODELS,LEVEL-3
	4	DESIGN FLOW CIRCUIT PROCEDURES
3rd	1	VLSI DESIGN FLOW
	2	Y-CHART
	3	DESIGN HIERARCHY
	4	VLSI DESIGN STYLES-FPGA,GATE ARRAY DESIGN
4th	1	STANDARD CELL BASED DESIGN STYLE,FULL CUSTOM DESIGN STYLE
	2	**2.FABRICATION OF MOSFET**
	3	BASIC STEPS IN FABRICATION PROCESS FLOW
	4	FABRICATION PROCESS OF NMOS TRANSISTOR
5th	1	FABRICATION PROCESS OF NMOS TRANSISTOR
	2	CMOS N-WELL FABRICATION PROCESS FLOW
	3	CMOS N-WELL FABRICATION PROCESS FLOW
	4	MOS FABRICATION PROCESS BY N-WELL ON P-SUBTRATE
6th	1	REVISION
	2	CMOS FABRICATION PROCESS BY P-WELL ON N-SUBTRATE
	3	LAYOUT DESIGN RULES
	4	STICK DIAGRAMS OF CMOS INVERTER
7th	1	**3.MOS INVERTER** BASIC NMOS INVERTERS
	2	WORKING OF RESISTIVE-LOAD INVERTER
	3	INVERTER WITH N-TYPE MOSFET LOAD-ENHANCEMENT LOAD
	4	DEPLETION NMOS INVERTER
8th	1	CIRCUIT OPERATION OF CMOS INVERTER
	2	CHARACTERSTICS AND INTERCONNECT EFFECTS OF CMOS INVERTER,DELAY TIME DEFINATIONS
	3	CMOS INVERTER DESIGN WITH DELAY CONSTRAINTS-TWO SAMPLE MASK LAY OUT FOR P-TYPE SUBTRATE
	4	**4.STATIC COMBINATIONAL,S EQUENTIAL,DYANA MICS LOGIC CIRCUITS AND MEMORIES** DEFINE STATIC COMBINATIONAL LOGIC,WORKING OF STATIC CMOS LOGIC CIRCUITS (TWO -INPUT NAND GATE)
9th	1	CMOS LOGIC CIRCUITS(NAND2 GATE)
	2	CMOS TRANSMISSION GATES(PASS GATE)
	3	BASICS OF COMPLEX LOGIC CIRCUITS,CLASSIFICATION OF LOGIC CIRCUITS BASED ON THEIR TEMPORAL BEHAVIOUR
	4	SR FLIP LATCH CIRCUIT,CLOCKED SR LATCH WORKING

10th	1	CMOS D LATCH OPERATION
	2	INTRODUCTION TO MICROPROCESSOR AND
	3	BASIC PRINCIPLES OF DYANAMIC PASS TRANSISTOR CIRCUITS;DYNAMIC RAM,SRAM
	4	OPERATION OF FLASH MEMORY
11th	1	REVISION
	2	**5.SYSTEM DESIGN METHOD AND SYNTHESIS** DESIGN LANGUAGE(SPL AND HDL) AND EDA TOOLS
	3	VHDL AND PACKAGE XLINX
	4	DESIGN STRATEGIES AND CONCEPT OF FPGA WITH STANDARD CELL BASED DESIGN
12th	1	VHDL FOR DESIGN SYNTHESIS USING CPLD OR FPGA
	2	BASIC IDEA OF RASPBERRY PI
	3	**6.INTRODUCTION TO EMBEDDED SYSTEMS**
	4	CHARACTERSTICS OF EMBEDDED SYSTEMS
13th	1	DIGIAL CAMERA-COMPONENTS AND OPERATION
	2	EMBEDDED SYSTEM TECHNOLOGIES-TECHNOLOGY FOR EMBEDDED SYSTEMS
	3	PROCESSOR TECHNOLOGY,IC TECHNOLOGY
	4	DESIGN TECHNOLOGY-PROCESSOR TECHNOLOGY
14th	1	GENERAL PURPOSE PROCESSORS-SOFTWARE
	2	BASIC ARCHITECTURE OF SINGLE PURPOSE PROCESSORS-HARDWARE
	3	APPLICATION-SPECIFIC PROCESSORS,MICROCONTROLLERS,DIGITAL SIGNAL PROCESSORS(DSP)
	4	IC TECHNOLOGY-FULL CUSTOM/VLSI
15th	1	SEMI CUSTOM ASIC(GATE ARRAY AND STANDARD CELL)
	2	OPERATION OF PROGRAMMABLE LOGIC DEVICE(PLD)
	3	BASIC IDEA OF ARDUINO MICROCONTROLLER
	4	REVISION

Signature of the Lecturer

Signature of the H.O.D.

Signature of the Principal