

PNS SCHOOL OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

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| Branch: CS Engg. | Semester: 3 rd | Name of the Lecturer: Aditya Narayan Jena |
| Subject: DECO | Classes Alloted in a Week: 4 | Duration of Semester: 14.07.2025 - 15.11.2025 |
| Week | Class Day | Theory / Practical Topic |
| 1st | 1 | INTRODUCTION TO DIGITAL ELECTRONICS: Analog signal,Digital signal |
| | 2 | Binary,Octal,Decimal,Hexadecimal number system |
| | 3 | Number system conversion |
| | 4 | Number system conversion |
| 2nd | 1 | Number system conversion |
| | 2 | Binary Arithemtic |
| | 3 | Boolean Algebra |
| | 4 | Simplification using Laws and basic operations |
| 3rd | 1 | LOGIC GATES & CIRCUITS: AND,OR,NOT gates |
| | 2 | NAND,NOR,XOR,XNOR Gates |
| | 3 | Design and Simplification of logic circuits using Boolean Algebra |
| | 4 | K-Map |
| 4th | 1 | K-Map |
| | 2 | K-Map |
| | 3 | Practical applications of logic gates in Real world |
| | 4 | COMBINATIONAL & SEQUENTIAL LOGIC CIRCUITS: MUX,DMUX |
| 5th | 1 | Encoder |
| | 2 | Decoder |
| | 3 | SR-FF |
| | 4 | JK FF |
| 6th | 1 | D FF,T FF |
| | 2 | Synchronous and Asynchronous counter |
| | 3 | Register |
| | 4 | Shift Register |
| 7th | 1 | Shift Register |
| | 2 | FUNDAMENTALS OF COMPUTER ORGANIZATION: Basic structure of a computer,CPU,Memory,Input/Output devices |
| | 3 | Fetch,Decode,Instruction cycle |
| | 4 | Types of Memory |
| 8th | 1 | Bus structure(A-bus,D-bus,C-bus) |
| | 2 | PROCESSOR ARCHITECTURE & CONTROL: Microprocessor and Microcontroller |
| | 3 | Basics of ALU |
| | 4 | Control Unit |
| 9th | 1 | Instruction Set Architecture |
| | 2 | RISC vs CISC |
| | 3 | Performance optimization in Processor |
| | 4 | I/O SYSTEMS and ADVANCED TOPICS: I/O devices and Interfaces |

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| 10th | 1 | I/O devices and Storage devices |
| | 2 | Interrupts |
| | 3 | DMA Technique |
| | 4 | Multicore Processor,GPUs |
| 11th | 1 | Embedded Systems |
| | 2 | Revision |
| | 3 | Revision |
| | 4 | Revision |

**Signature of the
Lecturer**

**Signature of the
H.O.D.**

**Signature of the
Principal**